Si823x 数据表

0.5 和 4.0 安培 ISOdriver（2.5 和 5 kV_{RMS}）

Si823x 隔离驱动器系列将两个独立、隔离的驱动器集成到一个封装内。Si8230/1/3/4 是高侧/低侧驱动器，而 Si8232/5/6/7/8 是双驱动器。可选峰值输出电流为 0.5 A（Si8230/1/2/7）和 4.0 A（Si8233/4/5/6/8）的版本。所有驱动器的最大供电电压为 24 V。

Si823x 驱动器采用 Silicon Labs 自主研发的硅隔离技术，提供符合 UL1577 的 5 kV_{RMS} 耐受电压以及 60 ns 快速传送时间。驱动器输出可连接到相同或独立的地线进行接地，或者连接到正或负电压。单个控制输入（Si8230/2/3/5/6/7/8）或 PWM 输入（Si8231/4）配置提供滞后大于 400 mV 的 TTL 级兼容输入。高度的集成、低传送延时、较小的外形及其灵活性和成本效益性使 Si823x 系列非常适合 MOSFET/IGBT 门驱动器隔离应用。

应用

- 供电系统
- 电机控制系统
- 直流到直流隔离供电
- 照明控制系统
- 等离子显示器
- 太阳能和工业变换器

安全认证

- UL 1577 认证
  - 1 分钟内最大 5000 Vrms
- CSA component notice 5A 认证
  - IEC 60950-1、61010-1、60601-1（强化绝缘）
- VDE 认证合规
  - IEC 60747-5-5（VDE 0884 第 5 部分）
  - EN 60950-1（强化绝缘）
- CQC 认证
  - GB4943.1

主要特点

- 两个完全隔离的驱动器集成在一个封装内
  - 最高 5 kV_{RMS} 输入到输出隔离
  - 驱动器到驱动器差分电压峰值为 1500 V_{DC}
- HS/LS 和双驱动器版本
- 最高 8 MHz 切换频率
- 0.5 A 峰值输出（Si8230/1/2/7）
- 4.0 A 峰值输出（Si8233/4/5/6/8）
- 高电磁抗扰度

1. 功能列表

Si823x 重要功能如下所列。

- 一个封装内两个完全隔离的驱动器：
  - 最高 5 kV_{RMS} 输入到输出隔离
  - 最高 1500 $V_{直流}$ 峰值驱动器到驱动器差分电压
- HS/LS 和双驱动器版本
- 最高 8 MHz 切换频率
- 0.5 A 峰值输出 (Si8230/1/2/7)
- 4.0 A 峰值输出 (Si8233/4/5/6/8)
- 高电磁抗扰度
- 60 ns 传送延时（最大）
- 独立 HS 和 LS 输入或 PWM 输入版本
- 瞬态抗扰度 > 45 kV/µs
- 重叠保护和可编程死区时间
- AEC-Q100 认证
- 宽工作范围：
  - －40 至 +125 ° C
- 符合 RoHS 的封装：
  - SOIC-16 宽体
  - SOIC-16 窄体
  - LGA-14

2. 订购指南

Table 2.1. Si823x Ordering Guide [1, 2]

Ordering Part Number (OPN)	Inputs	Configuration	Peak Current	UVLO Voltage	Isolation Rating	Temp Range	Package Type	Legacy Ordering Part Number (OPN) 2.5 kV Only
Wide Body (WB) Package Options								
Si8230BB-D-IS	VIA, VIB	High Side/ Low Side	0.5 A	8 V	2.5 kVrms	-40 to +125 °C	SOIC-16 Wide Body	Si8230-A-IS
Si8231BB-D-IS	PWM	High Side/ Low Side						Si8231-A-IS
Si8232BB-D-IS	VIA,VIB	Dual Driver						Si8232-A-IS
Si8234CB-D-IS	PWM	High Side/ Low Side	4.0 A	10 V				N/A
Si8233BB-D-IS	VIA,VIB	High Side/ Low Side		8 V				Si8233-B-IS
Si8234BB-D-IS	PWM	High Side/ Low Side						Si8234-B-IS
Si8235BB-D-IS	VIA,VIB	Dual Driver						Si8235-B-IS
Si8230AB-D-IS	VIA, VIB	High Side/ Low Side	0.5 A	5 V	2.5 kVrms	-40 to +125 °C	SOIC-16 Wide Body	N/A
Si8231AB-D-IS	PWM							N/A
Si8232AB-D-IS	VIA,VIB	Dual Driver						N/A
Si8233AB-D-IS	VIA,VIB	High Side/ Low Side	4.0 A	5 V				N/A
Si8234AB-D-IS	PWM							N/A
Si8235AB-D-IS	VIA,VIB	Dual Driver						N/A
Narrow Body (NB) Package Options								
Si8230BB-D-IS1	VIA,VIB	High Side/ Low Side	0.5 A	8 V	2.5 kVrms	-40 to +125 °C	SOIC-16 Narrow Body	N/A
Si8231BB-D-IS1	PWM	High Side/ Low Side						
Si8232BB-D-IS1	VIA,VIB	Dual Driver						
Si8233BB-D-IS1	VIA,VIB	High Side/ Low Side	4.0 A	8 V				
Si8234BB-D-IS1	PWM	High Side/ Low Side						
Si8235BB-D-IS1	VIA,VIB	Dual Driver						
Si8235BA-D-IS1	VIA,VIB	Dual Driver			1.0 kVrms			

Ordering Part Number (OPN)	Inputs	Configuration	Peak Current	UVLO Voltage	Isolation Rating	Temp Range	Package Type	Legacy Ordering Part Number (OPN) 2.5 kV Only
Si8230AB-D-IS1	VIA, VIB	High Side/ Low Side	0.5 A	5 V	2.5 kVrms	-40 to +125 °C	SOIC-16 Narrow Body	N/A
Si8231AB-D-IS1	PWM							N/A
Si8232AB-D-IS1	VIA, VIB	Dual Driver						N/A
Si8233AB-D-IS1	VIA, VIB	High Side/ Low Side	4.0 A	5 V				N/A
Si8234AB-D-IS1	PWM							N/A
Si8235AB-D-IS1	VIA, VIB	Dual Driver						N/A
LGA Package Options								
Si8233CB-D-IM	VIA, VIB	High Side/ Low Side	4.0 A	10 V	2.5 kVrms	-40 to +125 °C	LGA-14 5x5 mm	N/A
Si8233BB-D-IM				8 V				Si8233-B-IM
Si8233AB-D-IM				5 V				N/A
Si8234BB-D-IM	PWM			8 V				Si8234-B-IM
Si8234AB-D-IM				5 V				N/A
Si8235BB-D-IM	VIA, VIB	Dual Driver		8 V				Si8235-B-IM
Si8235AB-D-IM				5 V				N/A
Si8236BA-D-IM				8 V	1.0 kVrms		LGA-14 5x5 mm with Thermal Pad	Si8236-B-IM
Si8236AA-D-IM				5 V				N/A
5 kV Ordering Options								
Si8230BD-D-IS	VIA, VIB	High Side/ Low Side	0.5 A	8 V	5.0 kVrms	-40 to +125 °C	SOIC-16 Wide Body	N/A
Si8231BD-D-IS	PWM	High Side/ Low Side						
Si8232BD-D-IS	VIA, VIB	Dual Driver						
Si8233BD-D-IS	VIA, VIB	High Side/ Low Side	4.0 A					
Si8234BD-D-IS	PWM	High Side/ Low Side						
Si8235BD-D-IS	VIA, VIB	Dual Driver						
Si8230AD-D-IS	VIA, VIB	High Side/ Low Side	0.5 A	5 V	5.0 kVrms	-40 to +125 °C	SOIC-16 Wide Body	N/A
Si8231AD-D-IS	PWM							N/A
Si8232AD-D-IS	VIA, VIB	Dual Driver						N/A
Si8233AD-D-IS	VIA, VIB	High Side/ Low Side	4.0 A	5 V				N/A
Si8234AD-D-IS	PWM							N/A
Si8235AD-D-IS	VIA, VIB	Dual Driver						N/A
3 V VDDI Ordering Options								

Ordering Part Number (OPN)	Inputs	Configuration	Peak Current	UVLO Voltage	Isolation Rating	Temp Range	Package Type	Legacy Ordering Part Number (OPN) 2.5 kV Only
Si8237AB-D-IS1	VIA, VIB	Dual Driver	0.5 A	5 V	2.5 kVrms	-40 to +125 ° C	SOIC-16 Narrow Body	N/A
Si8237BB-D-IS1	VIA, VIB	Dual Driver		8 V				
Si8238AB-D-IS1	VIA, VIB	Dual Driver	4.0 A	5 V				
Si8238BB-D-IS1	VIA, VIB	Dual Driver		8 V				
Si8237AD-D-IS	VIA, VIB	Dual Driver	0.5 A	5 V	5.0 kVrms		SOIC-16 Wide Body	
Si8237BD-D-IS	VIA, VIB	Dual Driver		8 V				
Si8238AD-D-IS	VIA, VIB	Dual Driver	4.0 A	5 V				
Si8238BD-D-IS	VIA, VIB	Dual Driver		8 V				

1. All packages are RoHS-compliant with peak reflow temperatures of 260 ° C according to the JEDEC industry standard classifications and peak solder temperatures.
2. “Si” and “SI” are used interchangeably.

3. 系统概述

3.1 顶层方框图

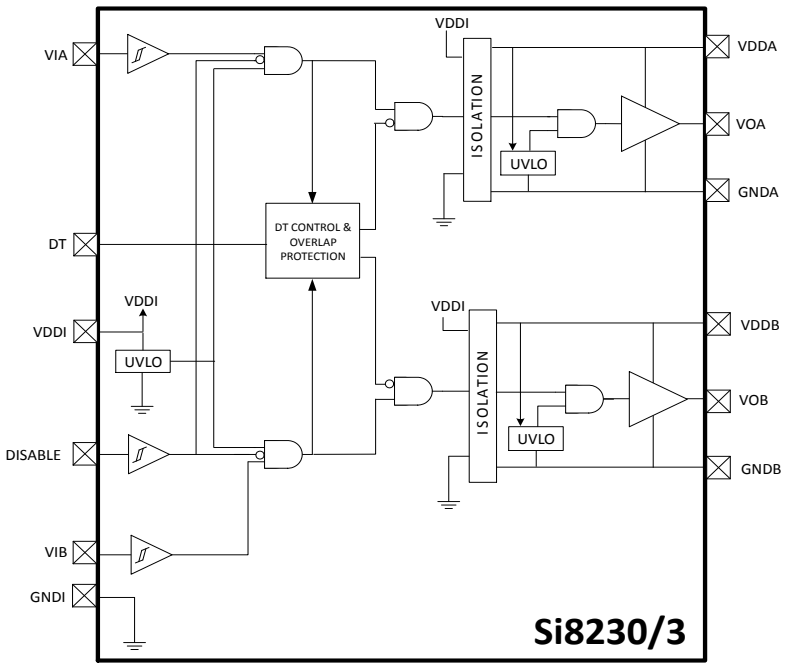


Figure 3.1. Si8230/3 双输入高侧 / 低侧隔离驱动器

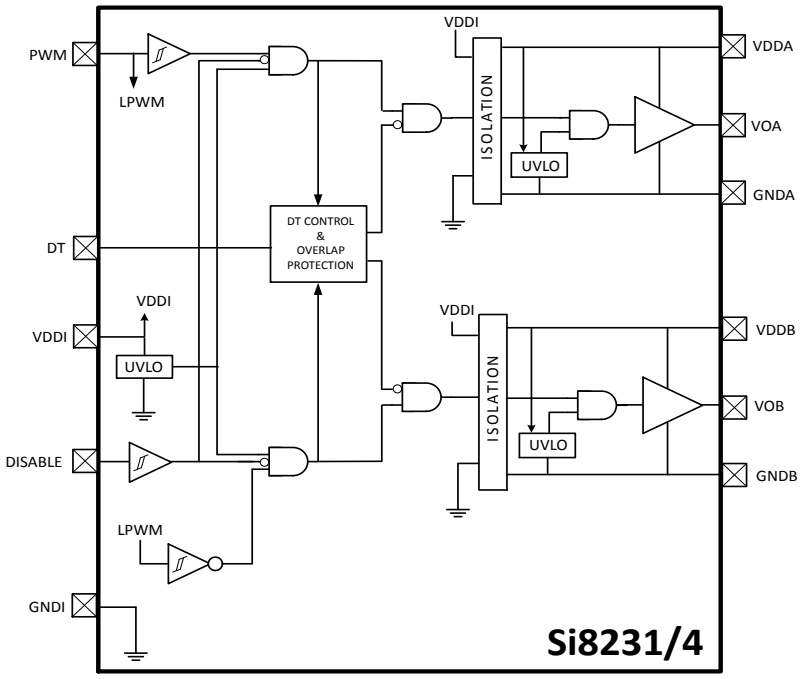


Figure 3.2. Si8231/4 单输入高侧 / 低侧隔离驱动器

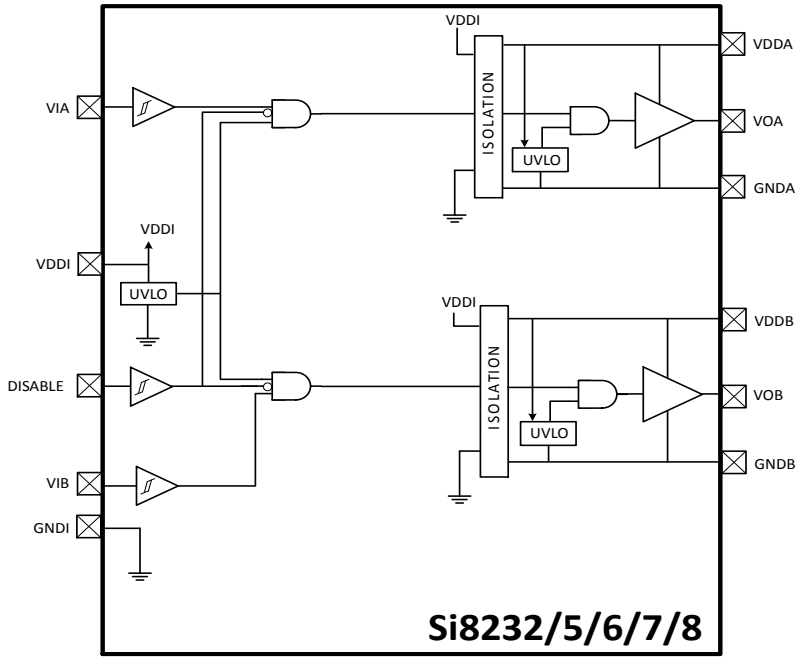


Figure 3.3. Si8232/5/6/7/8 双隔离驱动器

3.2 功能描述

Si823x 通道的工作情况与光电耦合器和门驱动器类似，但调制的是 RF 载波而不是光。这种简单的结构提供了一个牢靠的隔离数据路径，并且不要求有特别注意事项，或要求启动时初始化。一个 Si823x 通道的简化方框图如下图所示。

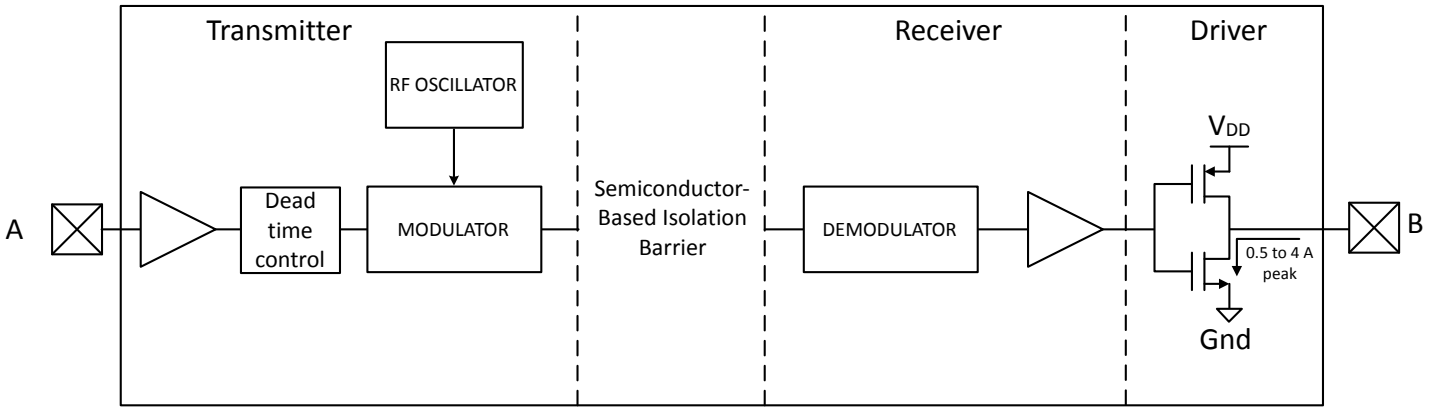


Figure 3.4. 简化通道示意图

一个通道包含由基于半导体的隔离屏障所分隔的一个 RF 发射器和一个 RF 接收器。对于发射器，输入 A 对 RF 振荡器利用开/关键控提供的载波进行调制。接收器含一个解调器，根据 RF 内部能量对输入状态进行解码，并通过输出驱动器将结果应用到输出 B。这种 RF 开/关键控方式优于脉冲代码方式，因其能够提供最佳的噪音抑制、低能耗和更好的磁场抑制。请参阅下图以了解详情。

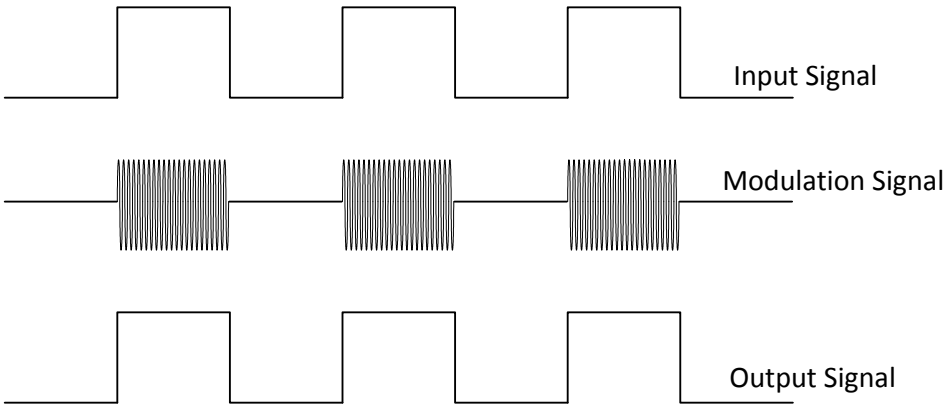


Figure 3.5. 调制方式

3.3 典型工作特征（0.5 安培）

Figure 3.6 相对于供电电压的上升/下降时间 on page 8 至 Figure 3.15 相对于温度的输出源电流 on page 9 中描述的典型性能特性仅供参考。实际规格限值见 Table 4.1 Electrical Characteristics[1] on page 21。

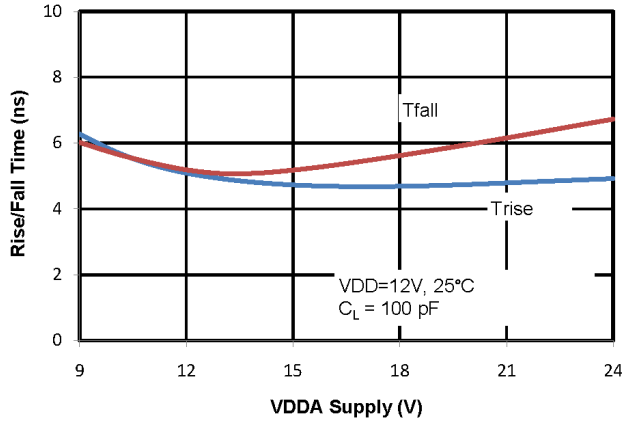


Figure 3.6. 相对于供电电压的上升/下降时间

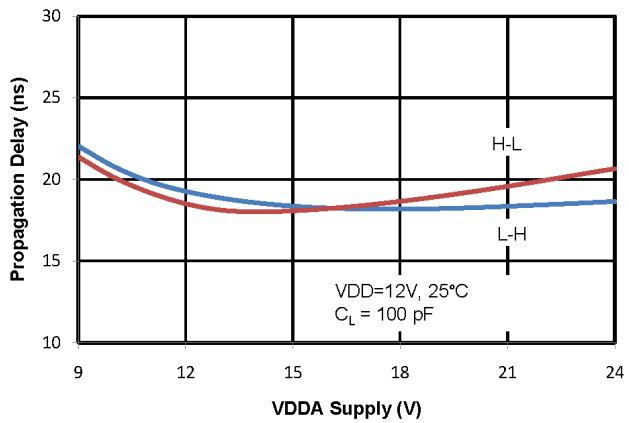


Figure 3.7. 相对于供电电压的传送延时

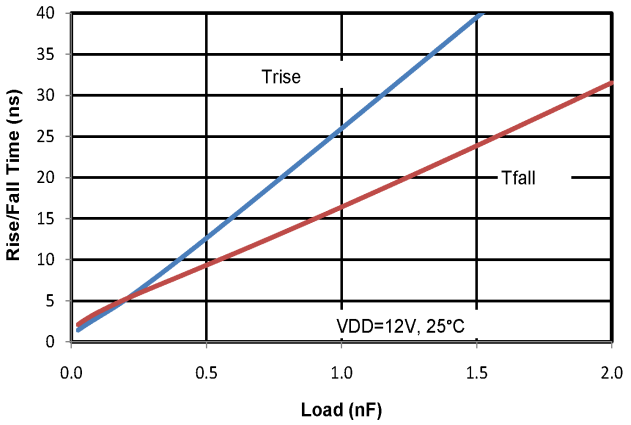


Figure 3.8. 相对于负荷的上升/下降时间

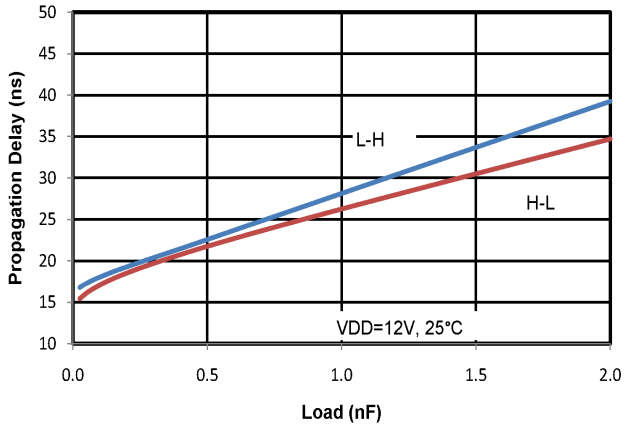


Figure 3.9. 相对于负荷的传送延时

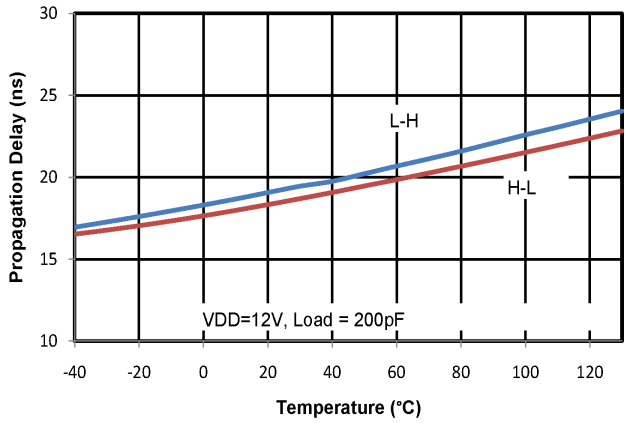


Figure 3.10. 相对于温度的传送延时

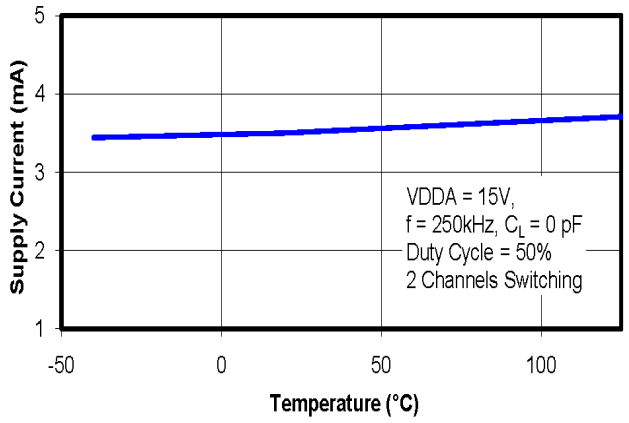


Figure 3.11. 相对于温度的供电电流

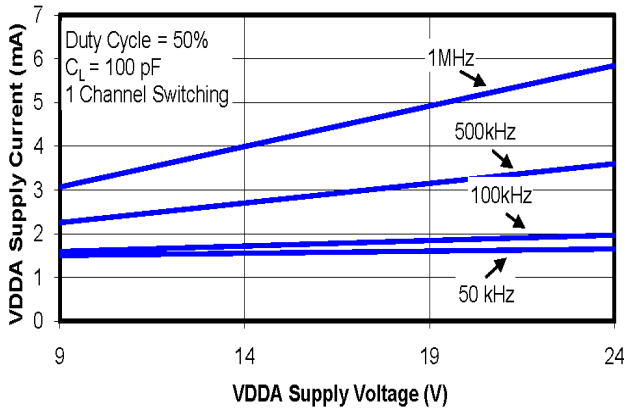


Figure 3.12. 相对于供电电压的供电电流

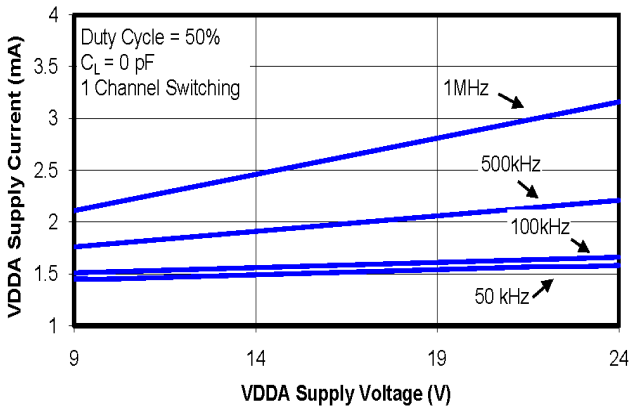


Figure 3.13. 相对于供电电压的供电电流

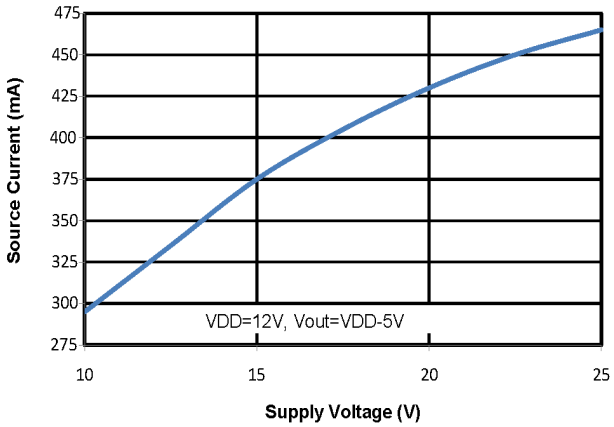


Figure 3.14. 相对于供电电压的输出源电流

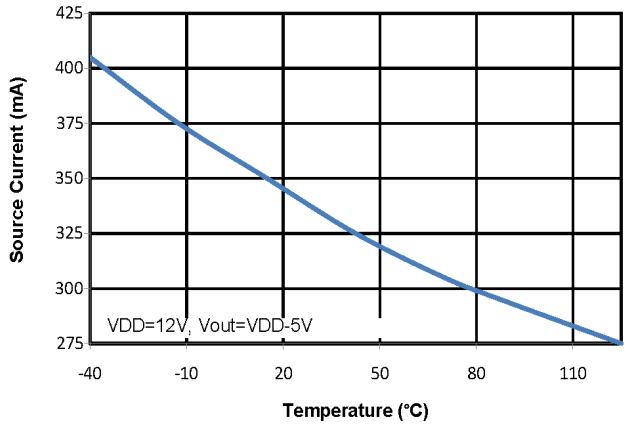


Figure 3.15. 相对于温度的输出源电流

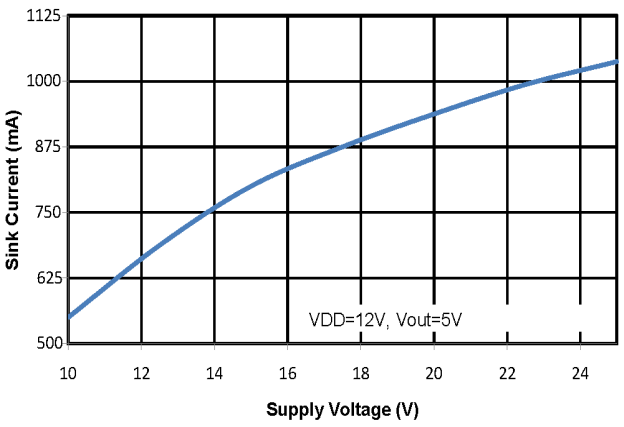


Figure 3.16. 相对于供电电压的输出吸入电流

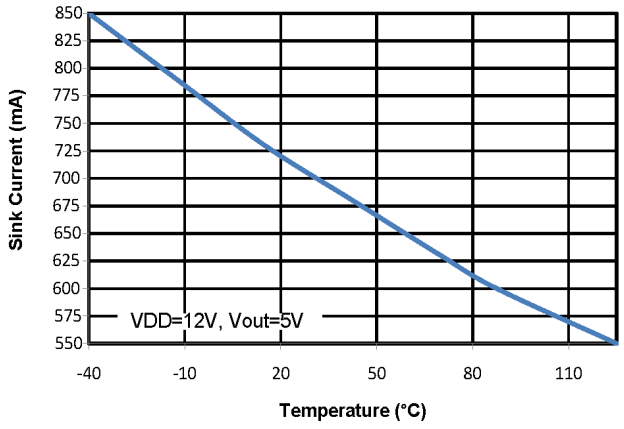


Figure 3.17. 相对于温度的输出吸入电流

3.4 典型工作特征（4.0 安培）

Figure 3.18 相对于供电电压的上升/下降时间 on page 10 至 Figure 3.27 相对于温度的输出源电流 on page 11 中描述的典型性能特性仅供参考。实际规格限值见 Table 4.1 Electrical Characteristics[1] on page 21。

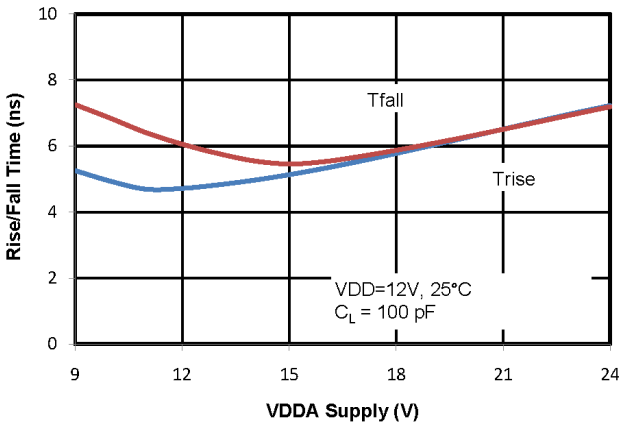


Figure 3.18. 相对于供电电压的上升/下降时间

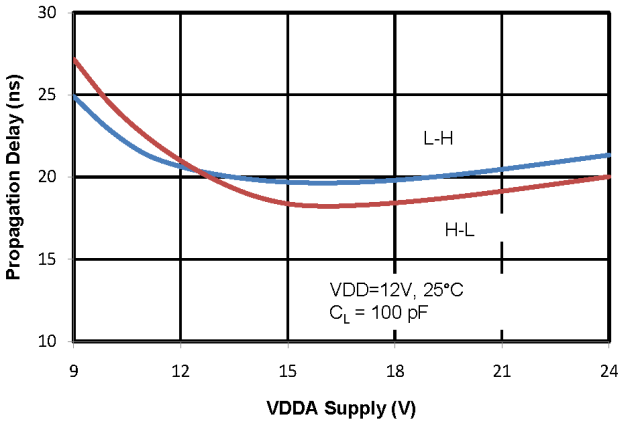


Figure 3.19. 相对于供电电压的传送延时

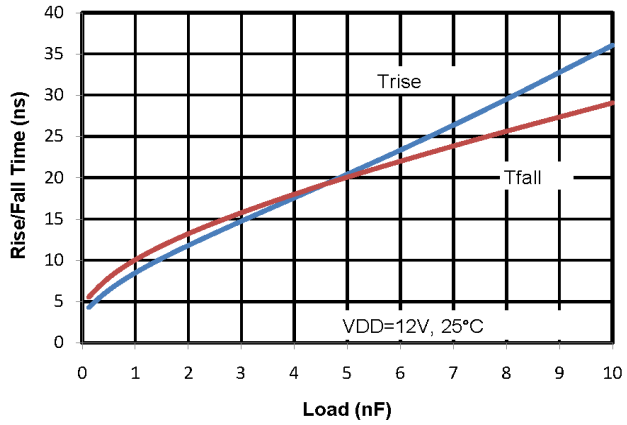


Figure 3.20. 相对于负荷的上升/下降时间

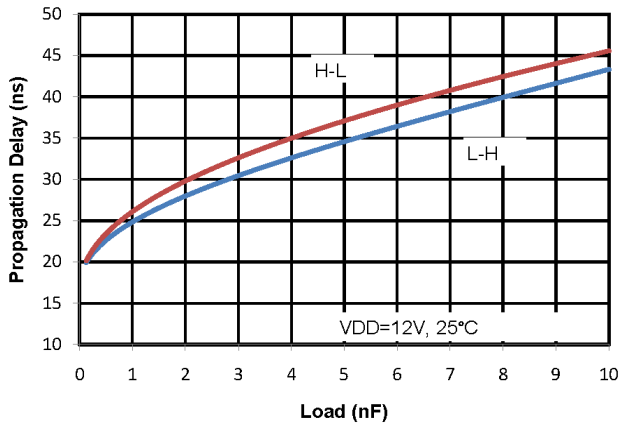


Figure 3.21. 相对于负荷的传送延时

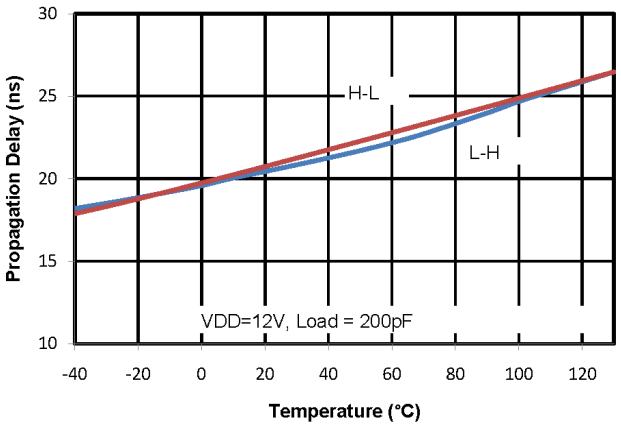


Figure 3.22. 相对于温度的传送延时

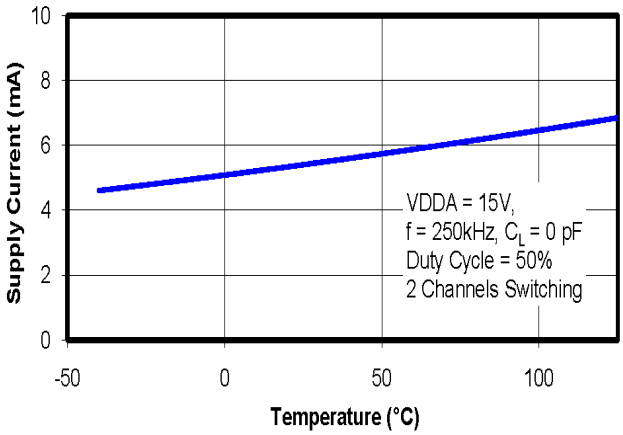


Figure 3.23. 相对于温度的供电电流

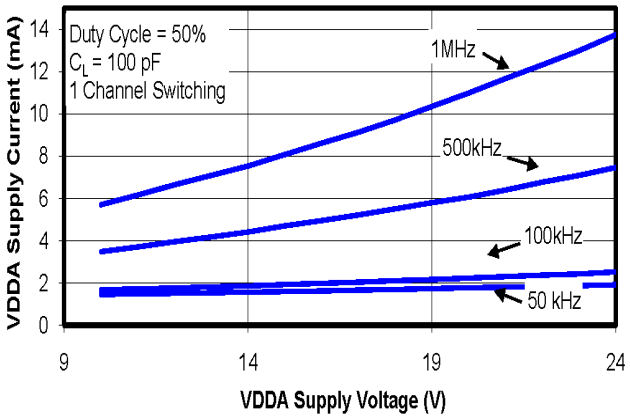


Figure 3.24. 相对于供电电压的供电电流

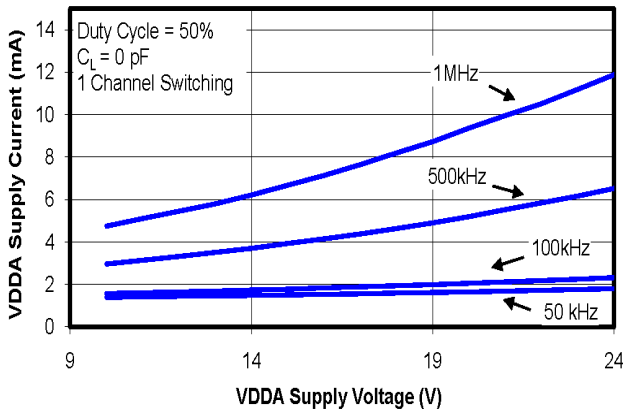


Figure 3.25. 相对于供电电压的供电电流

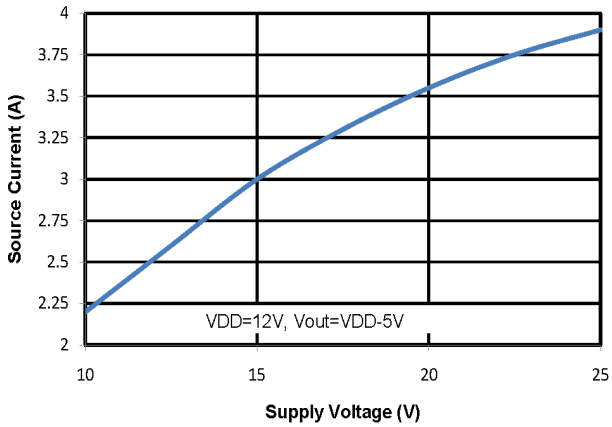


Figure 3.26. 相对于供电电压的输出源电流

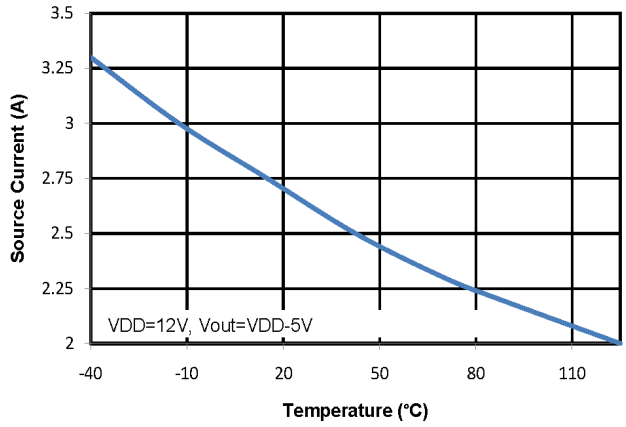


Figure 3.27. 相对于温度的输出源电流

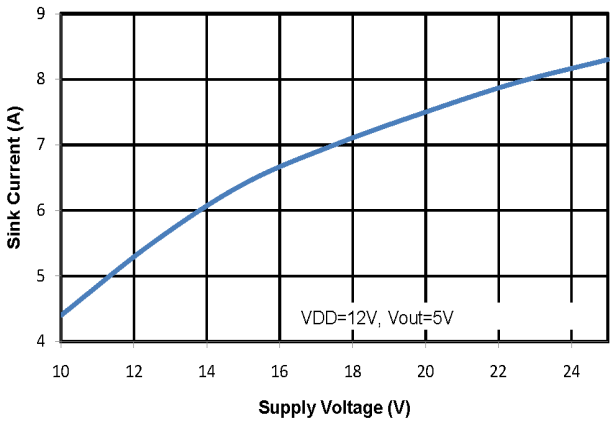


Figure 3.28. 相对于供电电压的输出吸入电流

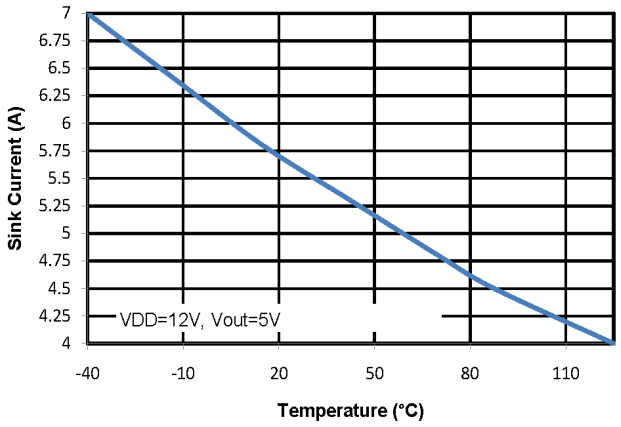


Figure 3.29. 相对于温度的输出吸入电流

3.5 系列简介和启动过程中的逻辑运算

Si823x 系列隔离驱动器包括高侧、低侧和双驱动器配置。

3.5.1 产品

下表显示本系列中各产品的配置和功能简介。

Table 3.1. Si823x Family Overview

Part Number	Configuration	Overlap Protection	Programmable Dead Time	Inputs	Peak Output Current (A)
Si8230	High-Side/Low-Side	√	√	VIA, VIB	0.5
Si8231	High-Side/Low-Side	√	√	PWM	0.5
Si8232/7	Dual Driver	—	—	VIA, VIB	0.5
Si8233	High-Side/Low-Side	√	√	VIA, VIB	4.0
Si8234	High-Side/Low-Side	√	√	PWM	4.0
Si8235/6/8	Dual Driver	—	—	VIA, VIB	4.0

3.5.2 器件行为

下表包含 Si8230/3、Si8231/4 和 Si8232/5/6 系列的真值表。

Table 3.2. Si823x Family Truth Table[1]

Si8230/3 (High-Side/Low-Side) Truth Table						
Inputs		VDDI State	Disable	Output		Notes
VIA	VIB			VOA	VOB	
L	L	Powered	L	L	L	Output transition occurs after internal dead time expires.
L	H	Powered	L	L	H	Output transition occurs after internal dead time expires.
H	L	Powered	L	H	L	Output transition occurs after internal dead time expires.
H	H	Powered	L	L	L	Invalid state. Output transition occurs after internal dead time expires.
X[2]	X[2]	Unpowered	X	L	L	Output returns to input state within 7 µs of VDDI power restoration.
X	X	Powered	H	L	L	Device is disabled.
Si8231/4 (PWM Input High-Side/Low-Side) Truth Table						
PWM Input		VDDI State	Disable	Output		Notes
				VOA	VOB	
H		Powered	L	H	L	Output transition occurs after internal dead time expires.
L		Powered	L	L	H	Output transition occurs after internal dead time expires.
X[2]		Unpowered	X	L	L	Output returns to input state within 7 µs of VDDI power restoration.
X		Powered	H	L	L	Device is disabled.
Si8232/5/6/7/8 (Dual Driver) Truth Table						
Inputs		VDDI State	Disable	Output		Notes
VIA	VIB			VOA	VOB	
L	L	Powered	L	L	L	Output transition occurs immediately (no internal dead time).
L	H	Powered	L	L	H	Output transition occurs immediately (no internal dead time).
H	L	Powered	L	H	L	Output transition occurs immediately (no internal dead time).
H	H	Powered	L	H	H	Output transition occurs immediately (no internal dead time).
X[2]	X[2]	Unpowered	X	L	L	Output returns to input state within 7 µs of VDDI power restoration.
X	X	Powered	H	L	L	Device is disabled.

Si8230/3 (High-Side/Low-Side) Truth Table
Notes: 1. This truth table assumes VDDA and VDDB are powered. If VDDA and VDDB are below UVLO, see 3.9 欠压锁定操作 for more information. 2. Note that an input can power the input die through an internal diode if its source has adequate current.

3.6 供电连接

隔离要求强制 VDDI、VDDA 和 VDDB 单独供电。这些供电的去耦电容必须尽可能靠近 Si823x 的 VDD 和 GND 引脚。这些电容器的最佳值取决于负荷电流以及芯片和为其供电的调节器之间的距离。推荐低效串联电阻式 (ESR) 电容器，例如钽电容。

3.7 功率耗散考虑

正确的系统设计必须确保在整个负荷范围内 Si823x 在安全热限值内工作。Si823x 总功耗散为偏压电源电流、内部寄生切换耗损以及系列门电阻和负荷的功耗之和。公式 1 显示了 Si823x 总功耗散。

$$P_D = (V_{DDI})(I_{DDI}) + 2(I_{DD2})(V_{DD2}) + \left(f\right)\left(Q_{TL}\right)\left(V_{DD2}\right)\left[\frac{R_p}{R_p + R_g}\right] + \left(f\right)\left(Q_{TL}\right)\left(V_{DD2}\right)\left[\frac{R_p}{R_p + R_g}\right] + 2fCintV_{DD2}{}^2$$

其中：

P_D 是 Si823x 器件的总功耗散 (W)

I_{DDI} 是输入端最大偏置电流 (3 mA)

I_{DD2} 是驱动器芯片最大偏置电流 (2.5 mA)

C_{int} 是内部寄生电容（对于 0.5 A 驱动器为 75 pF，对于 4.0 A 驱动器为 370 pF）

VDDI 是输入侧 VDD 供电电压（2.7 至 5.5 V）

V_{DD2} 是驱动器端供电电压（10 至 24 V）

f 是切换频率 (Hz)

Q_{TL} 是被驱动的 FET 的栅极电荷

R_G 是外部门电阻

R_P 是驱动器上拉开关的 $R_{DS(ON)}$：（对于 0.5 A 驱动器，Rp = 15 Ω 对于 4.0 A 驱动器，Rp = 2.7 Ω

R_n 是驱动器下拉开关的 $R_{DS(ON)}$：（对于 0.5 A 驱动器，Rn = 5 Ω 对于 4.0 A 驱动器，Rn = 1 Ω

Equation 1

0.5 A 驱动器功耗示例（使用方程式 1 并给出以下事项）：

V_{DDI} = 5.0 V

V_{DD2} = 12 V

f = 350 kHz

R_G = 22 Ω

Q_G = 25 nC

$$Pd = 0.015 + 0.060 + \left(350 \times 10^3\right)\left(25 \times 10^{-9}\right)\left(12\right)\left[\frac{5}{5 + 22}\right] + 2\left[\left(350 \times 10^3\right)\left(75 \times 10^{-12}\right)(144)\right] = 145\,\text{mW}$$

通过上式使用公式 2 计算驱动器结点温度，其中：

Pd 是 Si823x 器件的总功耗散 (W)

θja 是从结点到空气的热阻（在此例中为 105 ° C/W）

T_A 是环境温度

$$T_j = P_d \times \Theta_{ja} \times T_A = (0.145)(105) + 20 = 35.2^oC$$

Si823x 允许的最大功耗散由封装热阻、环境温度和允许的最大结点温度决定，如公式 2 所示：

$$P_{Dmax} \leq \frac{T_{jmax} - T_A}{\Theta ja}$$

其中：

P_{Dmax} = Si823x 的最大功耗散 (W)

T_{jmax} = Si823x 的最大结点温度 (150 ° C)

T_A = 环境温度 (° C)

Θja = Si823x 的结点到空气热阻 (105 ° C/W)

f = Si823x 切换频率 (Hz)

Equation 2

将 P_{Dmax}、T_{jmax}、T_A 和 θ_{ja} 的值代入公式 2 中可得出允许的最大总功耗散 (1.19 W)。将此限值和 Table 4.1 Electrical Characteristics[1] on page 21 中的相应数据表值代入公式 1 中并进行简化，可找到允许的最大负荷。结果是公式 3（0.5 A 驱动器）和公式 4（4.0 A 驱动器），两者均假设 VDDI = 5 V 和 VDDA = VDDB = 18 V。

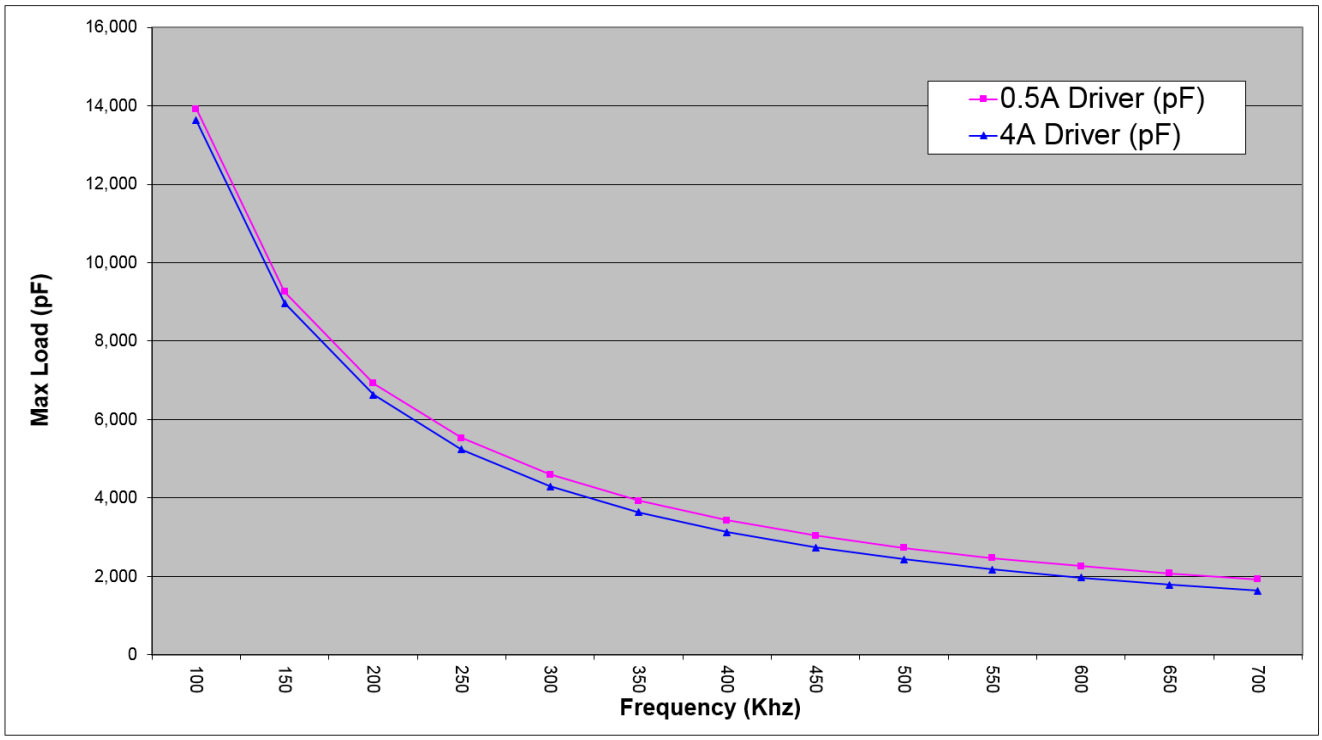
$$C_{L(MAX)} = \frac{1.4 \times 10^{-3}}{f} - 7.5 \times 10^{-11}$$

Equation 3

$$C_{L(MAX)} = \frac{1.4 \times 10^{-3}}{f} - 3.7 \times 10^{-10}$$

Equation 4

公式 3 和公式 4 在下图中以图表形式表示，其沿负荷线的点表示相应切换频率的 CL 封装损耗限值。



3.8 布局注意事项

最重要的是最大程度减少驱动器路径中的环路和 Si823x VDD 线路上的噪音。必须注意让 Si823x 尽可能靠近其驱动的器件才能最大程度减少这些路径中的寄生电感。另外，VDD 供电和接地轨迹路径必须尽可能短。为此，强烈推荐使用供电和接地平面。如采取用于供电器件和小信号元件的独立接地和 VDD 平面的分割接地平面系统，可提供最佳的整体降噪性能。

3.9 欠压锁定操作

启动、正常工作和关闭时的器件行为见 Figure 3.30 正常工作和关闭时的器件行为 on page 17，其中 UVLO+ 和 UVLO- 分别是正向和负向阈值。请注意，输出 VOA 和 VOB 在输入侧电源（VDDI）不存在时默认为低。

3.9.1 器件启动

输出 VOA 和 VOB 在启动中保持为低，直到 VDD 在时间段 tSTART 中高于 UVLO 阈值。之后，输出遵循输入 VIA 和 VIB 的状态。

3.9.2 欠压锁定

欠压锁定（UVLO）是为了器件启动和关闭时以及 VDD 低于规定的工作电路范围时防止错误操作。输入（控制）侧的驱动器 A 和驱动器 B 分别拥有自己的欠压锁定监控器。

Si823x 输入侧在 VDDI $\leq$ $VDDI_{UV-}$ 时进入 UVLO 状态，且在 VDDI > $VDDI_{UV+}$ 时退出。驱动器输出 VOA 和 VOB 在 Si823x 输入侧处于 UVLO 下时保持为低，且各自的 VDD 供电（VDDA、VDDB）在容差内。每个驱动器输出可独立进出 UVLO。例如，VOA 在 VDDA 低于 $VDDA_{UV-}$ 时无条件地进入 UVLO，在 VDDA 上升到高于 $VDDA_{UV+}$ 时退出 UVLO。

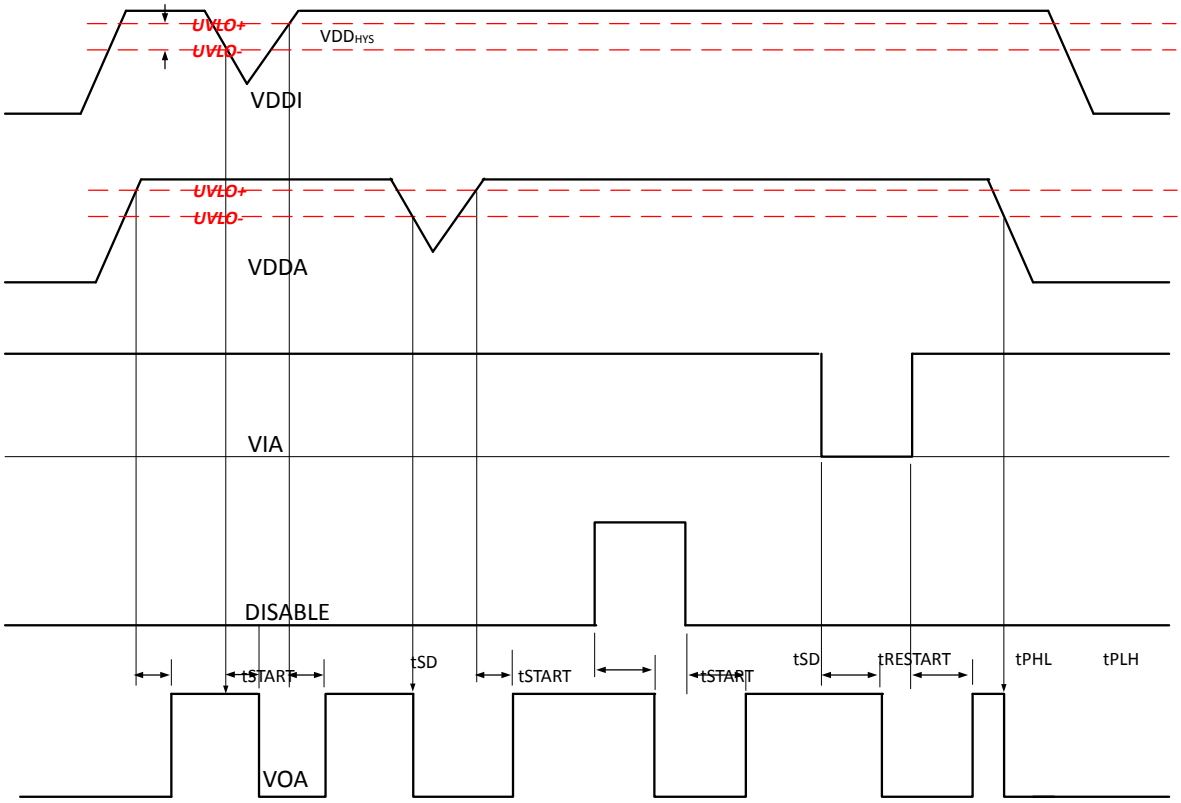


Figure 3.30. 正常工作和关闭时的器件行为

3.9.3 欠压锁定 (UVLO)

UVLO 电路在 VDD 低于锁定阈值时无条件驱动 VO 变为低。Figure 3.31 Si823x UVLO 响应 (5 V) on page 18 至 Figure 3.34 Si823x UVLO 响应 (12.5 V) on page 18 显示，在上电时 Si823x 保持在 UVLO 下直到 VDD 上升至高于 VDD_{UV+}。掉电时，Si823x 在 VDD 低于 UVLO 阈值加滞后（即 VDD ≤ VDD_{UV+} – VDD_{HYS}）时进入 UVLO。

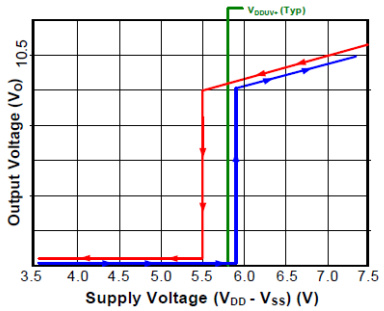


Figure 3.31. Si823x UVLO 响应 (5 V)

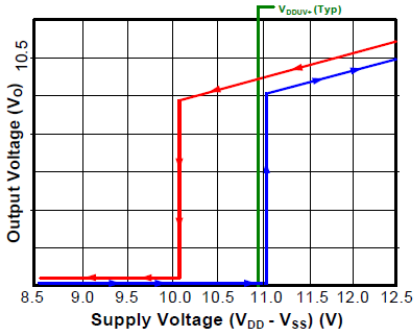


Figure 3.32. Si823x UVLO 响应 (10 V)

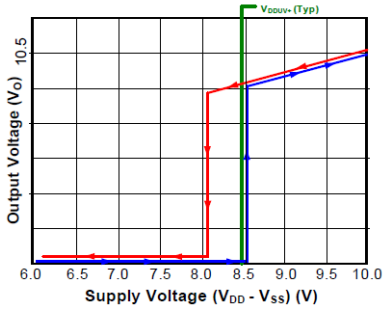


Figure 3.33. Si823x UVLO 响应 (8 V)

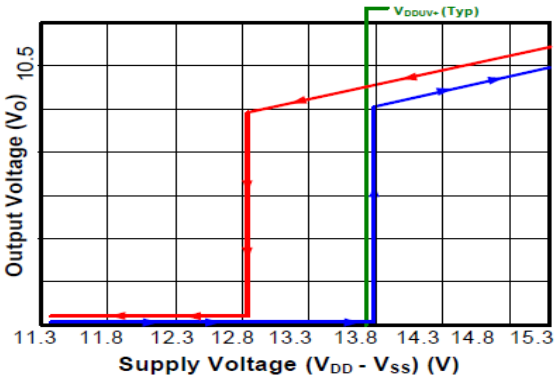


Figure 3.34. Si823x UVLO 响应 (12.5 V)

3.9.4 控制输入

VIA、VIB 和 PWM 输入是高真值、符合 TTL 电平的逻辑输入。VIA 和 VIB 上逻辑高信号引发相应的输出转为高。对于 PWM 输入版本 (Si8231/4) 来说，PWM 输入为高时，VOA 为高且 VOB 为低，而 PWM 输入为低时，VOA 为低且 VOB 为高。

3.9.5 禁用输入

在 DISABLE 输入变为高之后，将无条件驱动 VOA 和 VOB 变为低，无论 VIA 和 VIB 状态如何。在 DISABLE =V_{IH} 后，器件在 tSD 内停止工作，且在 DISABLE = V_{IL} 后于 tRESTART 内恢复。如果 VDDI 低于其 UVLO 水平（即 VOA、VOB 仍低），则 DISABLE 输入无效。

3.10 可编程死区时间和重叠保护

所有高侧/低侧驱动器 (Si8230/1/3/4) 都包括可编程重叠保护以防止输出 VOA 和 VOB 同时为高。这些器件也包括可编程死区时间，在 VOA 和 VOB 瞬态间添加了用户可编程的延时。启用后，死区时间应用于所有瞬态，即使是在重叠恢复后。按照公式 5，死区时间延时量 (DT) 由从 DT 输入接地的一个电阻 (RDT) 编程。请注意，死区时间引脚可连接到 VDDI 或保持浮动，以便在约 400 ps 下提供额定死区时间。

$$DT \approx 10 \times RDT$$

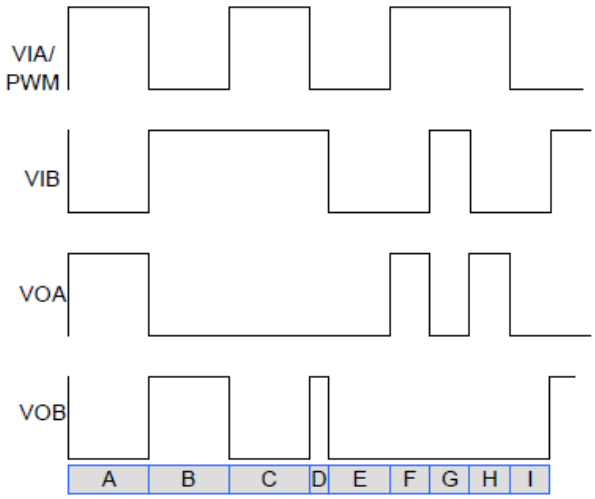
其中：

DT = 死区时间 (ns) 以及

RDT = 死区时间编程电阻 (kΩ)

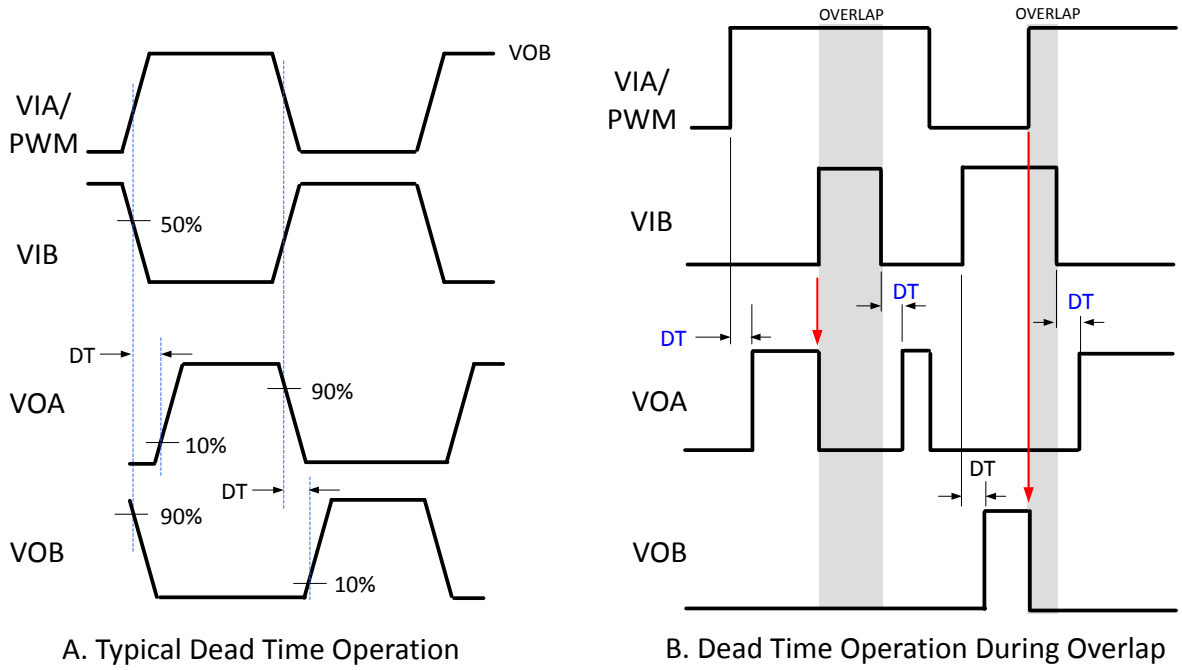
Equation 5

驱动 VIA 和 VIB 的器件应提供 TDD 最小死区时间以避免激活重叠保护。两个输入驱动器的输入/输出时间波形见 Figure 3.35 高侧/低侧双输入驱动器的输入/输出波形 on page 19，死区时间波形见 Figure 3.36 高侧/低侧双输入驱动器的死区时间波形 on page 20。



Ref	Description
A	Normal operation: VIA high, VIB low.
B	Normal operation: VIB high, VIA low.
C	Contention: VIA = VIB = high.
D	Recovery from contention: VIA transitions low.
E	Normal operation: VIA = VIB = low.
F	Normal operation: VIA high, VIB low.
G	Contention: VIA = VIB = high.
H	Recovery from contention: VIB transitions low.
I	Normal operation: VIB transitions high.

Figure 3.35. 高侧/低侧双输入驱动器的输入/输出波形



A. Typical Dead Time Operation

B. Dead Time Operation During Overlap

Figure 3.36. 高侧/低侧双输入驱动器的死区时间波形

4. 电气规格

Table 4.1. Electrical Characteristics[1]

2.7 V < VDDI < 5.5 V, VDDA = VDDB = 12 V or 15 V. TA = -40 to +125 °C. Typical specs at 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Specifications						
Input-side Power Supply Voltage	VDDI	Si8230/1/2/3/4/5/6	4.5	—	5.5	V
		Si8237/8	2.7	—	5.5	
Driver Supply Voltage	VDDA, VDDB	Voltage between VDDA and GNDA, and VDDB and GNDB (See 2. 订购指南)	6.5	—	24	V
Input Supply Quiescent Current	IDDI(Q)	Si8230/2/3/5/6/7/8	—	2	3	mA
		Si8231/4	—	3.5	5	mA
Output Supply Quiescent Current	IDDA(Q), IDDB(Q)	Current per channel	—	—	3.0	mA
Input Supply Active Current	IDDI	Input freq = 500 kHz, no load	—	3.5	—	mA
Output Supply Active Current	IDDA IDDB	Current per channel with Input freq = 500 kHz, no load	—	6	—	mA
Input Pin Leakage Current	IVIA, IVIB, IPWM		-10	—	+10	µA dc
Input Pin Leakage Current (Si8230/1/2/3/4/5/6)	IDISABLE		-10	—	+10	µA dc
Input Pin Leakage Current (Si8237/8)			-1000	+1000		
Logic High Input Threshold	VIH		2.0	—	—	V
Logic Low Input Threshold	VIL		—	—	0.8	V
Input Hysteresis	VI_{HYST}	Si8230/1/2/3/4/5/6/7/8	400	450	—	mV
Logic High Output Voltage	VOAH, VOBH	IOA, IOB = -1 mA	(VDDA / VDDB) — 0.04	—	—	V
Logic Low Output Voltage	VOAL, VOBL	IOA, IOB = 1 mA	—	—	0.04	V
Output Short-Circuit Pulsed Sink Current	IOA(SCL), IOB(SCL)	Si8230/1/2/7, Figure 4.1 IOL 吸收电流测试电路 on page 24	—	0.5	—	A
		Si8233/4/5/6/8, Figure 4.1 IOL 吸收电流测试电路 on page 24	—	4.0	—	A
Output Short-Circuit Pulsed Source Current	IOA(SCH), IOB(SCH)	Si8230/1/2/7, Figure 4.2 IOH 源电流测试电路 on page 24	—	0.25	—	A
		Si8233/4/5/6/8, Figure 4.2 IOH 源电流测试电路 on page 24	—	2.0	—	A

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Sink Resistance	$R_{ON(SINK)}$	Si8230/1/2/7	—	5.0	—	Ω
		Si8233/4/5/6/8	—	1.0	—	Ω
Output Source Resistance	$R_{ON(SOURCE)}$	Si8230/1/2/7	—	15	—	Ω
		Si8233/4/5/6/8	—	2.7	—	Ω
VDDI Undervoltage Threshold	$VDDI_{UV+}$	VDDI rising (Si8230/1/2/3/4/5/6)	3.60	4.0	4.45	V
VDDI Undervoltage Threshold	$VDDI_{UV-}$	VDDI falling (Si8230/1/2/3/4/5/6)	3.30	3.70	4.15	V
VDDI Lockout Hysteresis	$VDDI_{HYS}$	(Si8230/1/2/3/4/5/6)	—	250	—	mV
VDDI Undervoltage Threshold	$VDDI_{UV+}$	VDDI rising (Si8237/8)	2.15	2.3	2.5	V
VDDI Undervoltage Threshold	$VDDI_{UV-}$	VDDI falling (Si8237/8)	2.10	2.22	2.40	V
VDDI Lockout Hysteresis	$VDDI_{HYS}$	(Si8237/8)	—	75	—	mV
VDDA, VDDB Undervoltage Threshold	$VDDA_{UV+}$, $VDDB_{UV+}$	VDDA, VDDB rising				
5 V Threshold		See Figure 3.31 Si823x UVLO 响应 (5 V) on page 18.	5.20	5.80	6.30	V
8 V Threshold		See Figure 3.33 Si823x UVLO 响应 (8 V) on page 18.	7.50	8.60	9.40	V
10 V Threshold		See Figure 3.32 Si823x UVLO 响应 (10 V) on page 18.	9.60	11.1	12.2	V
12.5 V Threshold		See Figure 3.34 Si823x UVLO 响应 (12.5 V) on page 18.	12.4	13.8	14.8	V
VDDA, VDDB Undervoltage Threshold	$VDDA_{UV-}$, $VDDB_{UV-}$	VDDA, VDDB falling				
5 V Threshold		See Figure 3.31 Si823x UVLO 响应 (5 V) on page 18.	4.90	5.52	6.0	V
8 V Threshold		See Figure 3.33 Si823x UVLO 响应 (8 V) on page 18.	7.20	8.10	8.70	V
10 V Threshold		See Figure 3.32 Si823x UVLO 响应 (10 V) on page 18.	9.40	10.1	10.9	V
12.5 V Threshold		See Figure 3.34 Si823x UVLO 响应 (12.5 V) on page 18.	11.6	12.8	13.8	V
VDDA, VDDB Lockout Hysteresis	$VDDA_{HYS}$, $VDDB_{HYS}$	UVLO voltage = 5 V	—	280	—	mV
VDDA, VDDB Lockout Hysteresis	$VDDA_{HYS}$, $VDDB_{HYS}$	UVLO voltage = 8 V	—	600	—	mV
VDDA, VDDB Lockout Hysteresis	$VDDA_{HYS}$, $VDDB_{HYS}$	UVLO voltage = 10 V or 12.5 V	—	1000	—	mV
AC Specifications						
Minimum Pulse Width			—	10	—	ns
Propagation Delay	t_{PHL}, t_{PLH}	CL = 200 pF	—	30	60	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD		—	—	5.60	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Minimum Overlap Time[2]	TDD	DT = VDDI, No-Connect	—	0.4	—	ns
Programmed Dead Time[3]	DT	Figure 3.36 高侧/低侧双输入驱动器的死区时间波形 on page 20, RDT = 100 k	—	900	—	ns
		Figure 3.36 高侧/低侧双输入驱动器的死区时间波形 on page 20, RDT = 6 k	—	70	—	ns
Output Rise and Fall Time	t_R, t_F	C_L = 200 pF (Si8230/1/2/7)	—	—	20	ns
		C_L = 200 pF (Si8233/4/5/6/8)	—	—	12	ns
Shutdown Time from Disable True	t_{SD}		—	—	60	ns
Restart Time from Disable False	$t_{RESTART}$		—	—	60	ns
Device Start-up Time	t_{START}	Time from VDD_ = VDD_UV+ to VOA, VOB = VIA, VIB	—	—	40	µs
Common Mode Transient Immunity	CMTI	VIA, VIB, PWM = VDDI or 0 V V_{CM} = 1500 V (see Figure 4.3 共模瞬态抗扰度测试电路 on page 25)	20	45	—	kV/µs

Notes:

1. VDDA = VDDB = 12 V for 5, 8, and 10 V UVLO devices; VDDA = VDDB = 15 V for 12.5 V UVLO devices.
2. TDD is the minimum overlap time without triggering overlap protection (Si8230/1/3/4 only).
3. The largest RDT resistor that can be used is 220 kΩ.

4.1 测试电路

图 Figure 4.1 IOL 吸收电流测试电路 on page 24、Figure 4.2 IOH 源电流测试电路 on page 24 和 Figure 4.3 共模瞬态抗扰度测试电路 on page 25 分别对吸收电流、源电流和共模瞬态抗扰度测试电路进行了描述。

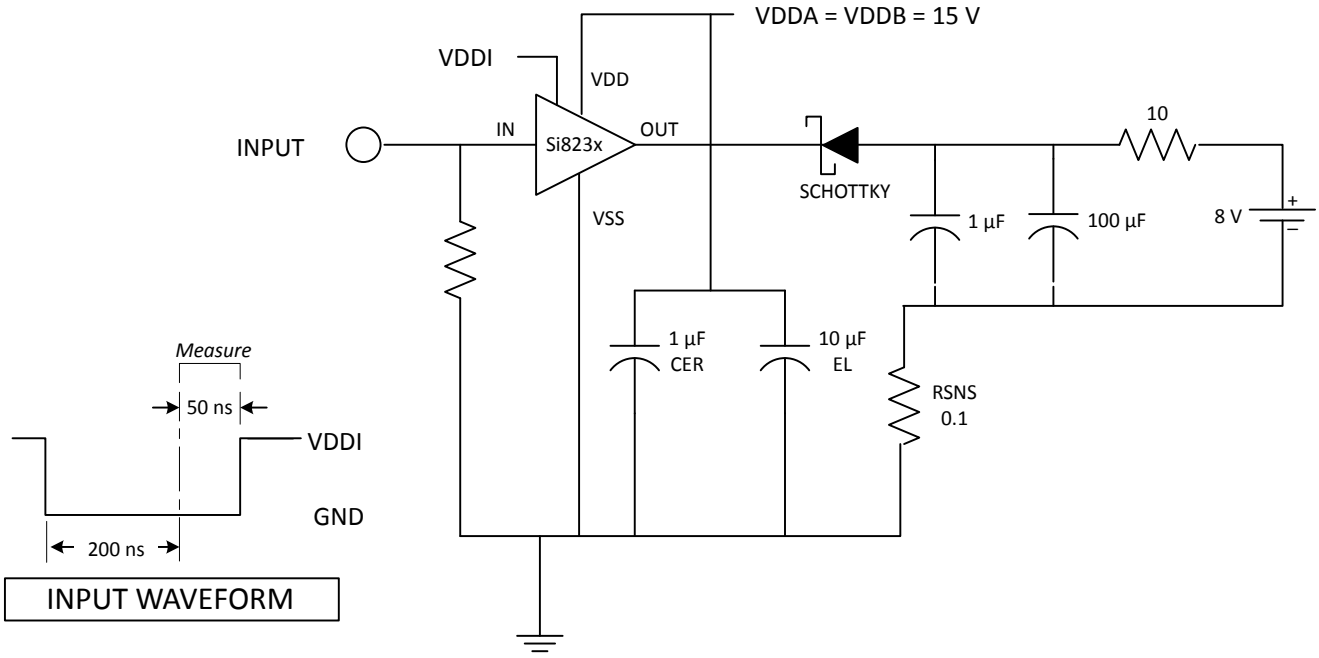


Figure 4.1. IOL 吸收电流测试电路

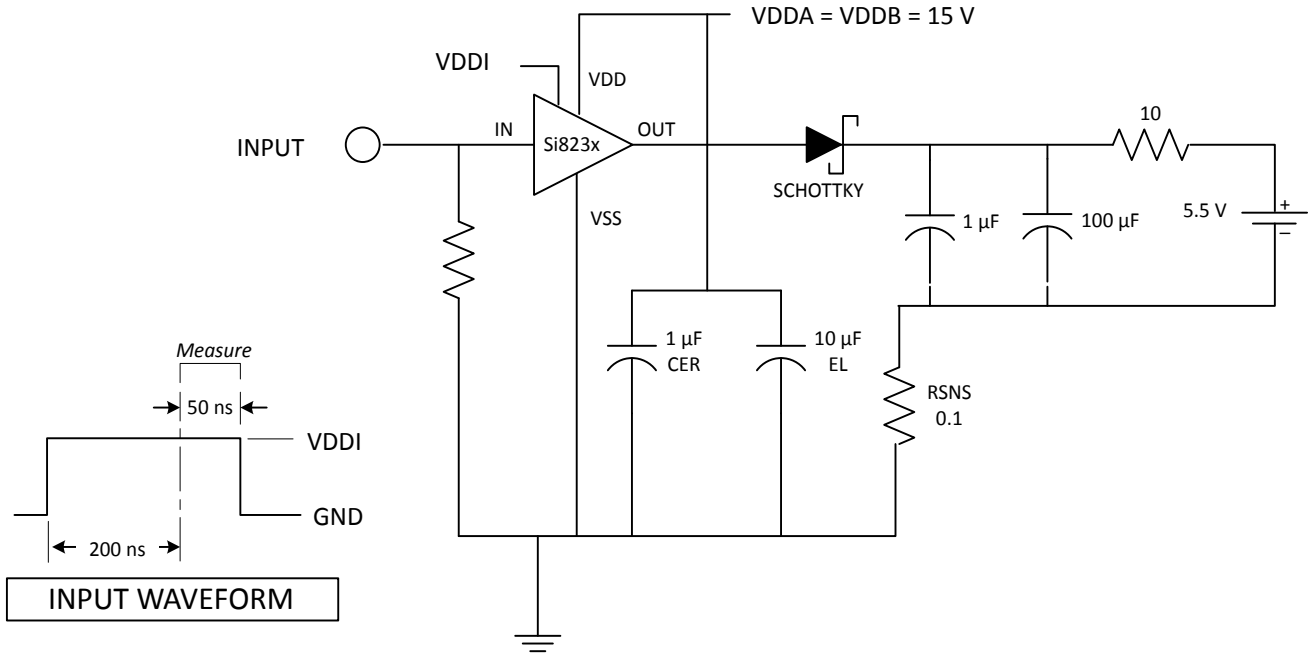


Figure 4.2. IOH 源电流测试电路

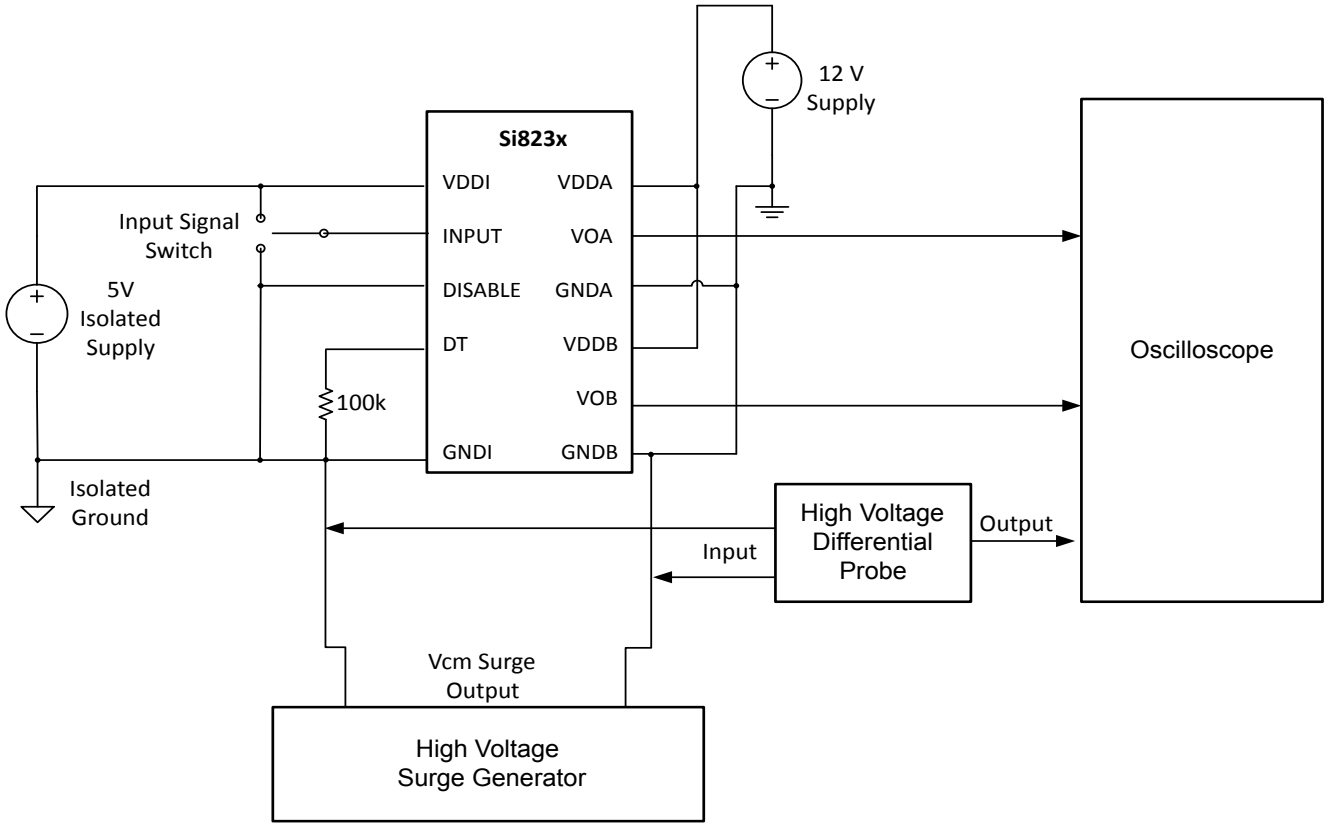


Figure 4.3. 共模瞬态抗扰度测试电路

Table 4.2. Regulatory Information[1, 2, 3, 4]

CSA
The Si823x is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
61010-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 600 V_{RMS} basic insulation working voltage.
60950-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
60601-1: Up to 125 V_{RMS} reinforced insulation working voltage; up to 380 V_{RMS} basic insulation working voltage.
VDE
The Si823x is certified according to IEC 60747-5-5. For more details, see File 5006301-4880-0001.
60747-5-5: Up to 891 V_{peak} for basic insulation working voltage.
60950-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
UL
The Si823x is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V_{RMS} isolation voltage for basic protection.
CQC
The Si823x is certified under GB4943.1-2011. For more details, see certificates CQC13001096106 and CQC13001096108.
Rated up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.

Notes:

1. Regulatory Certifications apply to 2.5 kV_{RMS} rated devices which are production tested to 3.0 kV_{RMS} for 1 sec.
2. Regulatory Certifications apply to 3.75 kV_{RMS} rated devices which are production tested to 4.5 kV_{RMS} for 1 sec.
3. Regulatory Certifications apply to 5.0 kV_{RMS} rated devices which are production tested to 6.0 kV_{RMS} for 1 sec.
4. For more information, see 2. 订购指南.

Table 4.3. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value				Unit
			WBSOIC-16 5 kV_{RMS}	WBSOIC-16 NBSOIC-16 2.5 kV_{RMS}	14 LD LGA 2.5 kV_{RMS}	14 LD LGA with Pad 1.0 kV_{RMS}	
Nominal Air Gap (Clearance)[1]	L(101)		8.0	8.0/4.01	3.5	1.75	mm
Nominal External Tracking (Creepage)[1]	L(102)		8.0	8.0/4.01	3.5	1.75	mm
Minimum Internal Gap (Internal Clearance)			0.014	0.014	0.014	0.014	mm
Tracking Resistance (Proof Tracking Index)	PTI	IEC60112	600	600	600	600	V
Erosion Depth	ED		0.019	0.019	0.021	0.021	mm
Resistance (Input-Output)[2]	R_{IO}		10^{12}	10^{12}	10^{12}	10^{12}	Ω
Capacitance (Input-Output)[2]	X_{IO}	f = 1 MHz	1.4	1.4	1.4	1.4	pF
Input Capacitance[3]	X_I		4.0	4.0	4.0	4.0	pF

Notes:

1. The values in this table correspond to the nominal creepage and clearance values as detailed in 7.1 封装外形：16 引脚宽体 SOIC, 7.2 封装外形：16 引脚窄体 SOIC, 7.3 封装外形：14 LD LGA (5 x 5 mm), and 7.4 封装外形：14 LD LGA 及导热垫 (5 x 5 mm). VDE certifies the clearance and creepage limits as 4.7 mm minimum for the NB SOIC-16 and 8.5 mm minimum for the WB SOIC-16 package. UL does not impose a clearance and creepage minimum for component level certifications. CSA certifies the clearance and creepage limits as 3.9 mm minimum for the NB SOIC 16 and 7.6 mm minimum for the WB SOIC-16 package.
2. To determine resistance and capacitance, the Si823x is converted into a 2-terminal device. Pins 1－8 (1-7, 14 LD LGA) are shorted together to form the first terminal and pins 9－16 (8-14, 14 LD LGA) are shorted together to form the second terminal. The parameters are then measured between these two terminals.
3. Measured from input pin to ground.

Table 4.4. IEC 60664-1 (VDE 0884 Part 5) Ratings

Parameter	Test Condition	Specification			
		WB SOIC-16	NB SOIC-16	14 LD LGA	14 LD LGA with Pad
Basic Isolation Group	Material Group	I	I	I	I

Parameter	Test Condition	Specification			
		WB SOIC-16	NB SOIC-16	14 LD LGA	14 LD LGA with Pad
Installation Classification	Rated Mains Voltages < 150 V_{RMS}	I-IV	I-IV	I-IV	I-IV
	Rated Mains Voltages < 300 V_{RMS}	I-IV	I-III	I-III	I-III
	Rated Mains Voltages < 400 V_{RMS}	I-III	I-II	I-II	I-II
	Rated Mains Voltages < 600 V_{RMS}	I-III	I-II	I-II	I-I

Table 4.5. IEC 60747-5-5 Insulation Characteristics[1]

Parameter	Symbol	Test Condition	Characteristic			Unit
			WB SOIC-16	NB SOIC-16 14 LD LGA	14 LD LGA with Pad	
Maximum Working Insulation Voltage	V_{IORM}		891	560	373	V peak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	1671	1050	700	V peak
Transient Overvoltage	V_{IOTM}	t = 60 sec	6000	4000	2650	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	2	2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	$>10^9$	$>10^9$	Ω

***Note:**

1. Maintenance of the safety data is ensured by protective circuits. The Si823x provides a climate classification of 40/125/21.

Table 4.6. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	WB SOIC-16	NB SOIC-16	14 LD LGA	14 LD LGA with Pad	Unit
Case Temperature	T_S		150	150	150	150	° C

Parameter	Symbol	Test Condition	WB SOIC-16	NB SOIC-16	14 LD LGA	14 LD LGA with Pad	Unit
Safety Input Current	I_S	θ_{JA} = 100 ° C/W (WB SOIC-16), 105 ° C/W (NB SOIC-16, 14 LD LGA), 50 ° C/W (14 LD LGA with Pad) V_{DDI} = 5.5 V, V_{DDA} = V_{DDB} = 24 V, T_J = 150 ° C, T_A = 25 ° C	50	50	50	100	mA
Device Power Dissipation[2]	P_D		1.2	1.2	1.2	1.2	Ω

Notes:

1. Maximum value allowed in the event of a failure. Refer to the thermal derating curve in Figures Figure 4.4 WB SOIC-16、NB SOIC-16、14 LD LGA 的热降额曲线，依赖于符合 DIN EN 60747-5-5 的外壳温度安全限值 on page 29 and Figure 4.5 带导热垫 14 LD LGA 的热降额曲线，依赖于符合 DIN EN 60747-5-5 的外壳温度安全限值 on page 30.
2. The Si82xx is tested with V_{DDI} = 5.5 V, V_{DDA} = V_{DDB} = 24 V, T_J = 150 ºC, C_L = 100 pF, input 2 MHz 50% duty cycle square wave.

Table 4.7. Thermal Characteristics

Parameter	Symbol	WB SOIC-16	NB SOIC-16	14 LD LGA	14 LD LGA with Pad	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	100	105	105	50	° C/W

Table 4.8. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Unit
Storage Temperature[2]	T_{STG}	-65	+150	° C
Ambient Temperature under Bias	T_A	-40	+125	° C
Junction Temperature	T_J	—	+150	° C
Input-side Supply Voltage	VDDI	-0.6	6.0	V
Driver-side Supply Voltage	VDDA, VDDB	-0.6	30	V
Voltage on any Pin with respect to Ground	V_{IO}	-0.5	VDD + 0.5	V
Peak Output Current (t_{PW} = 10 µs, duty cycle = 0.2%) (0.5 Amp versions)	I_{OPK}	—	0.5	A
Peak Output Current (t_{PW} = 10 µs, duty cycle = 0.2%) (4.0 Amp versions)	I_{OPK}	—	4.0	A

Parameter	Symbol	Min	Max	Unit
Lead Solder Temperature (10 sec.)		—	260	° C
Maximum Isolation (Input to Output) (1 sec) WB SOIC-16		—	6500	V_{RMS}
Maximum Isolation (Output to Output) (1 sec) WB SOIC-16		—	2500	V_{RMS}
Maximum Isolation (Input to Output) (1 sec) NB SOIC-16		—	4500	V_{RMS}
Maximum Isolation (Output to Output) (1 sec) NB SOIC-16		—	2500	V_{RMS}
Maximum Isolation (Input to Output) (1 sec) 14 LD LGA without Thermal Pad		—	3850	V_{RMS}
Maximum Isolation (Output to Output) (1 sec) 14 LD LGA without Thermal Pad		—	650	V_{RMS}
Maximum Isolation (Input to Output) (1 sec) 14 LD LGA with Thermal Pad		—	1850	V_{RMS}
Maximum Isolation (Output to Output) (1 sec) 14 LD LGA with Thermal Pad	—	—	0	V_{RMS}

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. VDE certifies storage temperature from -40 to 150 ° C.

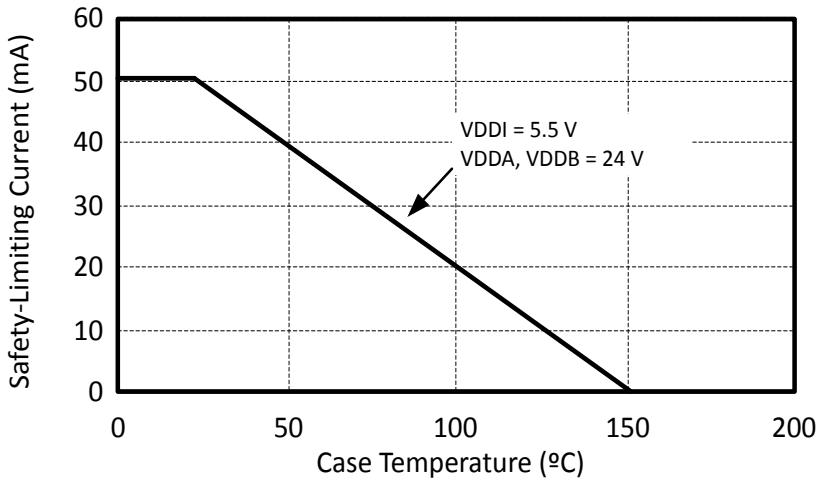


Figure 4.4. WB SOIC-16、NB SOIC-16、14 LD LGA 的热降额曲线，依赖于符合 DIN EN 60747-5-5 的外壳温度安全限值

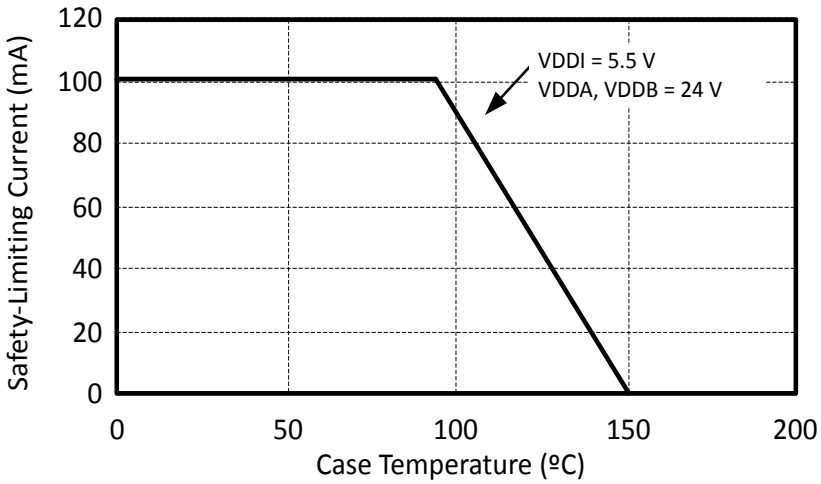


Figure 4.5. 带导热垫 14 LD LGA 的热降额曲线，依赖于符合 DIN EN 60747-5-5 的外壳温度安全限值

5. 应用

以下示例给出了使用 Si823x 的典型电路配置。

5.1 高侧 / 低侧驱动器

下图中的图 A 显示通过 VIA 和 VIB 输入信号实行控制的 Si8230/3，图 B 显示通过单个 PWM 信号实行控制的 Si8231/4。

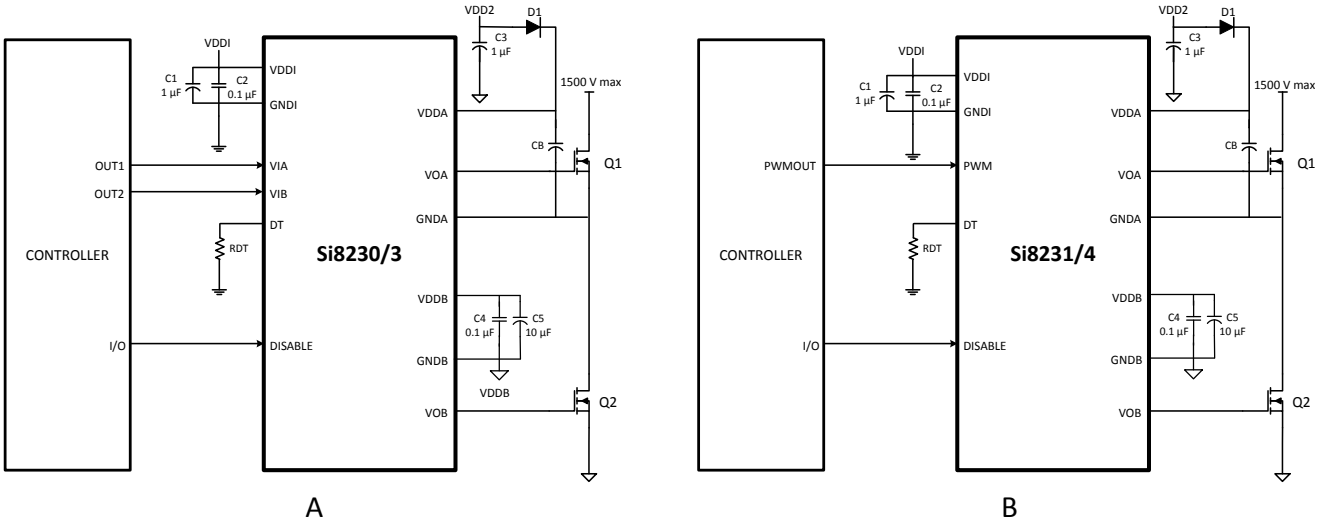


Figure 5.1. 半桥应用中的 Si823x

对于这两种应用来说，D1 和 CB 组成一个传统的自引导电路，允许 VOA 作为 Q1 的高侧驱动器工作，而 Q1 的最大漏电压为 1500 V。自引导启动时间取决于选择的 CB 电容。请参见应用说明“AN486：高侧自引导设计在供电系统中使用 Si823x ISOdrivers”。VOB 作为传统低侧驱动器连接，并且在大部分应用中，VDD2 与 VDDB 相同。请注意，Si823x 的输入侧要求 VDD 在 4.5 至 5.5 V 范围内（Si8237/8 则为 2.7 至 5.5 V 范围内），而 VDDA 和 VDDB 输出端供电必须根据各自的接地点在 6.5 至 24 V 之间。推荐在 Si823x 输入侧使用 0.1 和 1 µF 的旁路电容器，并且这些电容器应尽可能靠近芯片。另外，推荐在 Si823x 输出侧使用 0.1 和 10 µF 的旁路电容器，并且这些电容器应尽可能靠近芯片，以降低高频噪声并使性能最大化。

5.2 双驱动器

下图显示配置为双驱动器的 Si823x。注意，Q1 和 Q2 的漏电电压可引用于共同接地或不同接地，其间电压为 1500 V dc。

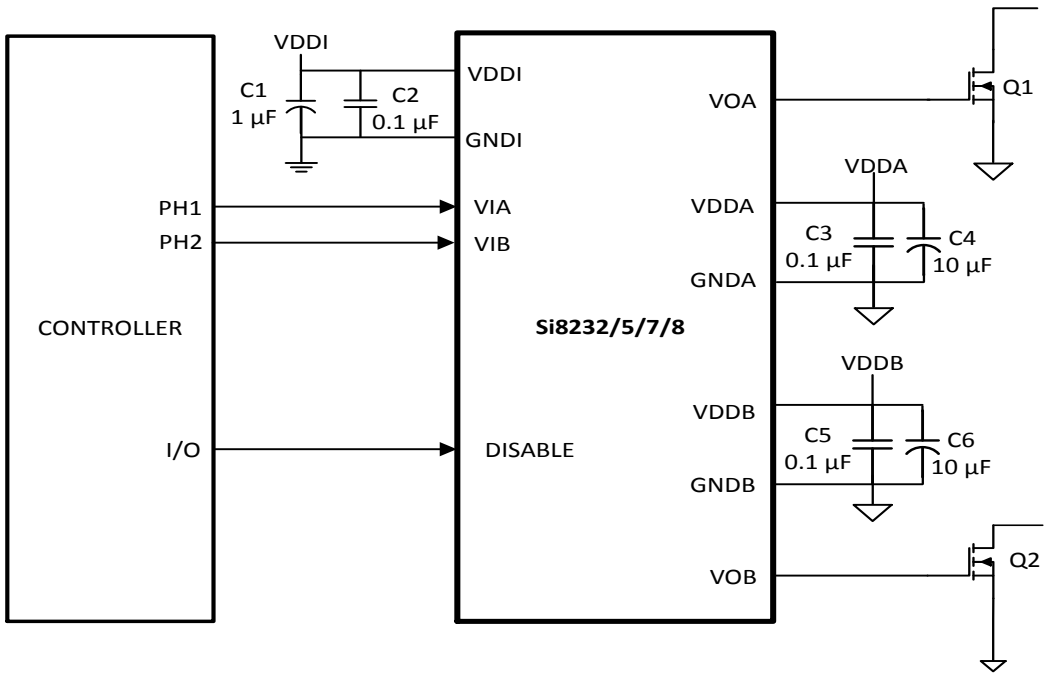


Figure 5.2. 双驱动器应用中的 Si8232/5/7/8

因为每个输出驱动器位于其自己的芯片上，所以 VOA 与 VOB 的相对电压极性可以交换而不损坏驱动器。也就是说，通过 VDD，VOA 的电压可以高于或低于 VOB 的电压而不损坏驱动器。因此，双驱动器低电位的高侧/低侧驱动程序可以使用 VOA 或 VOB 作为高侧驱动器。同样地，双驱动器能作为一个双低侧或双高侧驱动器运作，不会受静态或动态电压极性的变化影响。

5.3 双驱动器及热增强封装 (Si8236)

Si8236 的导热垫必须连接到散热器以降低热阻。一般来说，热屏障面积越大，热阻越低。推荐使用热 VIAS 为屏障增加体积。一般来说 VIAS 体积远大于屏障本身，且占用空间更少，从而更有效地降低热阻。虽然散热器一般不是电路接地点，但对于 Si8236 来说是一个很好的参考平面，且可作为降低 EMI 的屏障层。

Si8236 外层（包括 20 个热 VIAS）上有一个 10mm^2 的热平面，其热阻实测为 50 ° C/W。这比没有导热垫的 Si8235 改进很多。Si8235 的热阻实测为 105 ° C/W。此外应注意，Si8236 的 GNDA 和 GNDB 引脚通过导热垫连接在一起。

6. 引脚描述

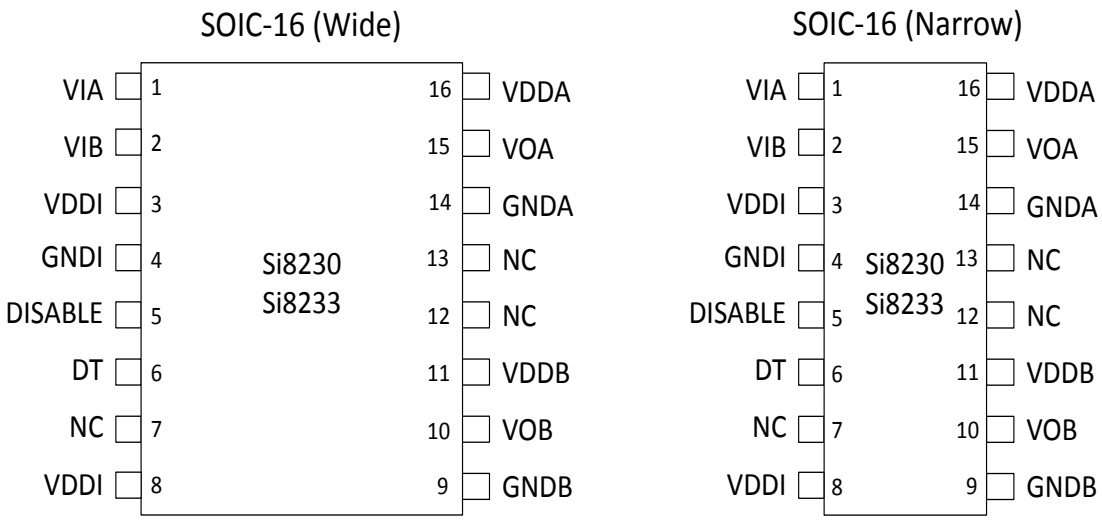


Table 6.1. Si8230/3 Two-Input HS/LS Isolated Driver (SOIC-16)

Pin	Name	Description
1	VIA	Non-inverting logic input terminal for Driver A.
2	VIB	Non-inverting logic input terminal for Driver B.
3	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
4	GNDI	Input-side ground terminal.
5	DISABLE	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
6	DT	Dead time programming input. The value of the resistor connected from DT to ground sets the dead time between output transitions of VOA and VOB. Defaults to 400 ps dead time when connected to VDDI or left open (see 3.10 可编程死区时间和重叠保护).
7	NC	No connection.
8	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
9	GNDB	Ground terminal for Driver B.
10	VOB	Driver B output (low-side driver).
11	VDDB	Driver B power supply voltage terminal; connect to a source of 6.5 to 24 V.
12	NC	No connection.
13	NC	No connection.
14	GNDA	Ground terminal for Driver A.
15	VOA	Driver A output (high-side driver).
16	VDDA	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.

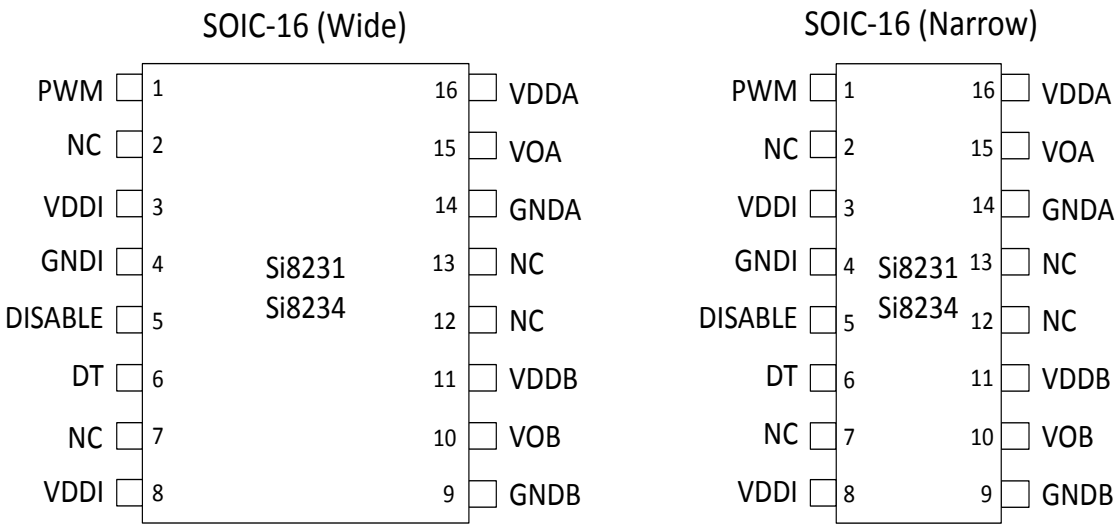


Table 6.2. Si8231/4 PWM Input HS/LS Isolated Driver (SOIC-16)

Pin	Name	Description
1	PWM	PWM input.
2	NC	No connection.
3	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
4	GNDI	Input-side ground terminal.
5	DISABLE	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
6	DT	Dead time programming input. The value of the resistor connected from DT to ground sets the dead time between output transitions of VOA and VOB. Defaults to 400 ps dead time when connected to VDDI or left open (see 3.10 可编程死区时间和重叠保护).
7	NC	No connection.
8	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
9	GNDB	Ground terminal for Driver B.
10	VOB	Driver B output (low-side driver).
11	VDDB	Driver B power supply voltage terminal; connect to a source of 6.5 to 24 V.
12	NC	No connection.
13	NC	No connection.
14	GNDA	Ground terminal for Driver A.
15	VOA	Driver A output (high-side driver).
16	VDDA	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.

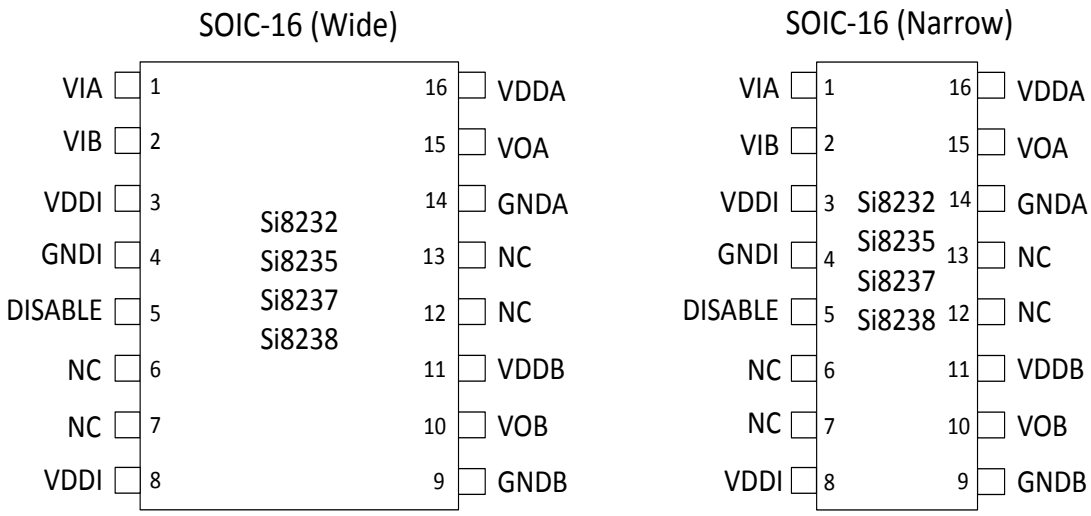


Table 6.3. Si8232/5/7/8 Dual Isolated Driver (SOIC-16)

Pin	Name	Description
1	VIA	Non-inverting logic input terminal for Driver A.
2	VIB	Non-inverting logic input terminal for Driver B.
3	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V, (2.7 to 5.5 V for Si8237/8).
4	GNDI	Input-side ground terminal.
5	DISABLE	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
6	NC	No connection.
7	NC	No connection.
8	VDDI	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V, (2.7 to 5.5 V for Si8237/8).
9	GNDB	Ground terminal for Driver B.
10	VOB	Driver B output.
11	VDDB	Driver B power supply voltage terminal; connect to a source of 6.5 to 24 V.
12	NC	No connection.
13	NC	No connection.
14	GNDA	Ground terminal for Driver A.
15	VOA	Driver A output.
16	VDDA	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.

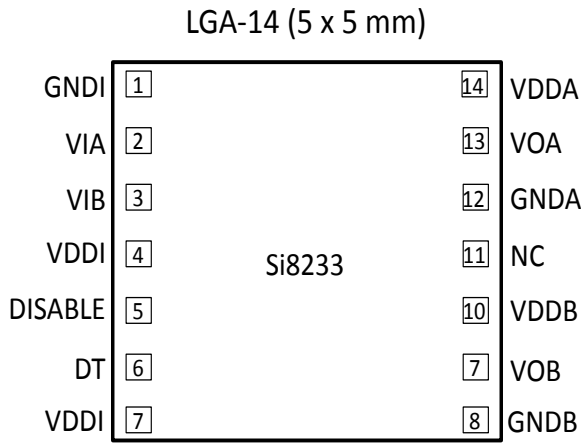


Table 6.4. Si8233 Two-Input HS/LS Isolated Driver (14 LD LGA)

Pin	Name	Description
GNDI	1	Input-side ground terminal.
VIA	2	Non-inverting logic input terminal for Driver A.
VIB	3	Non-inverting logic input terminal for Driver B.
VDDI	4	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
DISABLE	5	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
DT	6	Dead time programming input. The value of the resistor connected from DT to ground sets the dead time between output transitions of VOA and VOB. Defaults to 400 ps dead time when connected to VDDI or left open (see3.10 可编程死区时间和重叠保护).
VDDI	7	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
GNDB	8	Ground terminal for Driver B.
VOB	9	Driver B output (low-side driver).
VDDB	10	Driver B power supply voltage terminal; connect to a source of 6.5 to 24 V.
NC	11	No connection.
GNDA	12	Ground terminal for Driver A.
VOA	13	Driver A output (high-side driver).
VDDA	14	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.

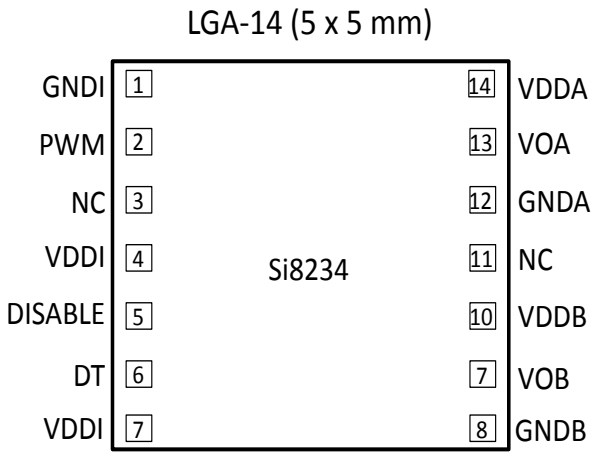


Table 6.5. Si8234 PWM Input HS/LS Isolated Driver (14 LD LGA)

Pin	Name	Description
GNDI	1	Input-side ground terminal.
PWM	2	PWM input.
NC	3	No connection.
VDDI	4	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
DISABLE	5	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
DT	6	Dead time programming input. The value of the resistor connected from DT to ground sets the dead time between output transitions of VOA and VOB. Defaults to 400 ps dead time when connected to VDDI or left open (see 3.10 可编程死区时间和重叠保护).
VDDI	7	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
GNDB	8	Ground terminal for Driver B.
VOB	9	Driver B output (low-side driver).
VDDB	10	Driver B power supply voltage terminal; connect to a source of 6.5 to 24 V.
NC	11	No connection.
GNDA	12	Ground terminal for Driver A.
VOA	13	Driver A output (high-side driver).
VDDA	14	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.

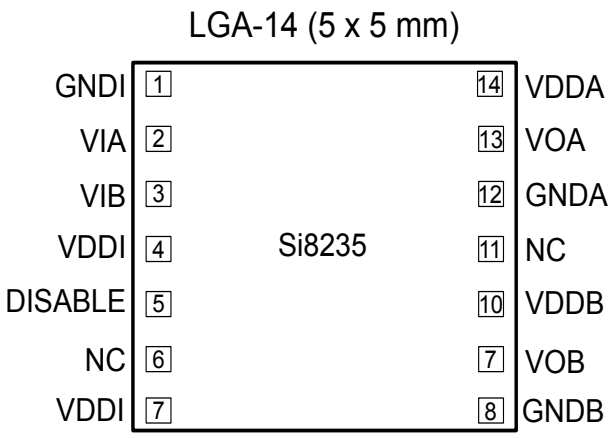


Table 6.6. Si8235 Dual Isolated Driver (14 LD LGA)

Pin	Name	Description
GNDI	1	Input-side ground terminal.
VIA	2	Non-inverting logic input terminal for Driver A.
VIB	3	Non-inverting logic input terminal for Driver B.
VDDI	4	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
DISABLE	5	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
NC	6	No connection.
VDDI	7	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
GNDB	8	Ground terminal for Driver B.
VOB	9	Driver B output (low-side driver).
VDDB	10	Driver B power supply voltage terminal; connect to a source of 6.5 to 24 V.
NC	11	No connection.
GNDA	12	Ground terminal for Driver A.
VOA	13	Driver A output (high-side driver).
VDDA	14	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.

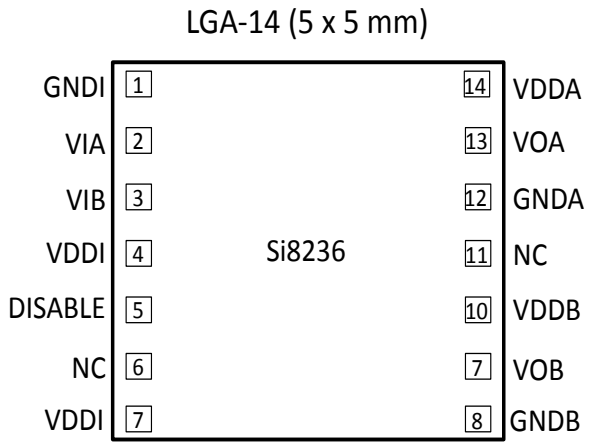


Table 6.7. Si8236 Dual Isolated Driver (14 LD LGA)

Pin	Name	Description
GNDI	1	Input-side ground terminal.
VIA	2	Non-inverting logic input terminal for Driver A.
VIB	3	Non-inverting logic input terminal for Driver B.
VDDI	4	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
DISABLE	5	Device Disable. When high, this input unconditionally drives outputs VOA, VOB LOW. It is strongly recommended that this input be connected to external logic level to avoid erroneous operation due to capacitive noise coupling.
NC	6	No connection.
VDDI	7	Input-side power supply terminal; connect to a source of 4.5 to 5.5 V.
GNDB	8	Ground terminal for Driver B. GNDA and GNDB pins for the Si8236 are connected together through the thermal pad.
VOB	9	Driver B output (low-side driver).
VDDB	10	Driver B power supply voltage terminal; connect to a source of 6.5 to 24 V.
NC	11	No connection.
GNDA	12	Ground terminal for Driver A. GNDA and GNDB pins for the Si8236 are connected together through the thermal pad.
VOA	13	Driver A output (high-side driver).
VDDA	14	Driver A power supply voltage terminal; connect to a source of 6.5 to 24 V.

7. 封装外形

7.1 封装外形：16 引脚宽体 SOIC

Figure 7.1 16 引脚宽体 SOIC on page 40 给出了 16 引脚宽体 SOIC 的 Si823x 封装细节。Table 7.1 Package Diagram Dimensions on page 40 列出了图示中尺寸的值。

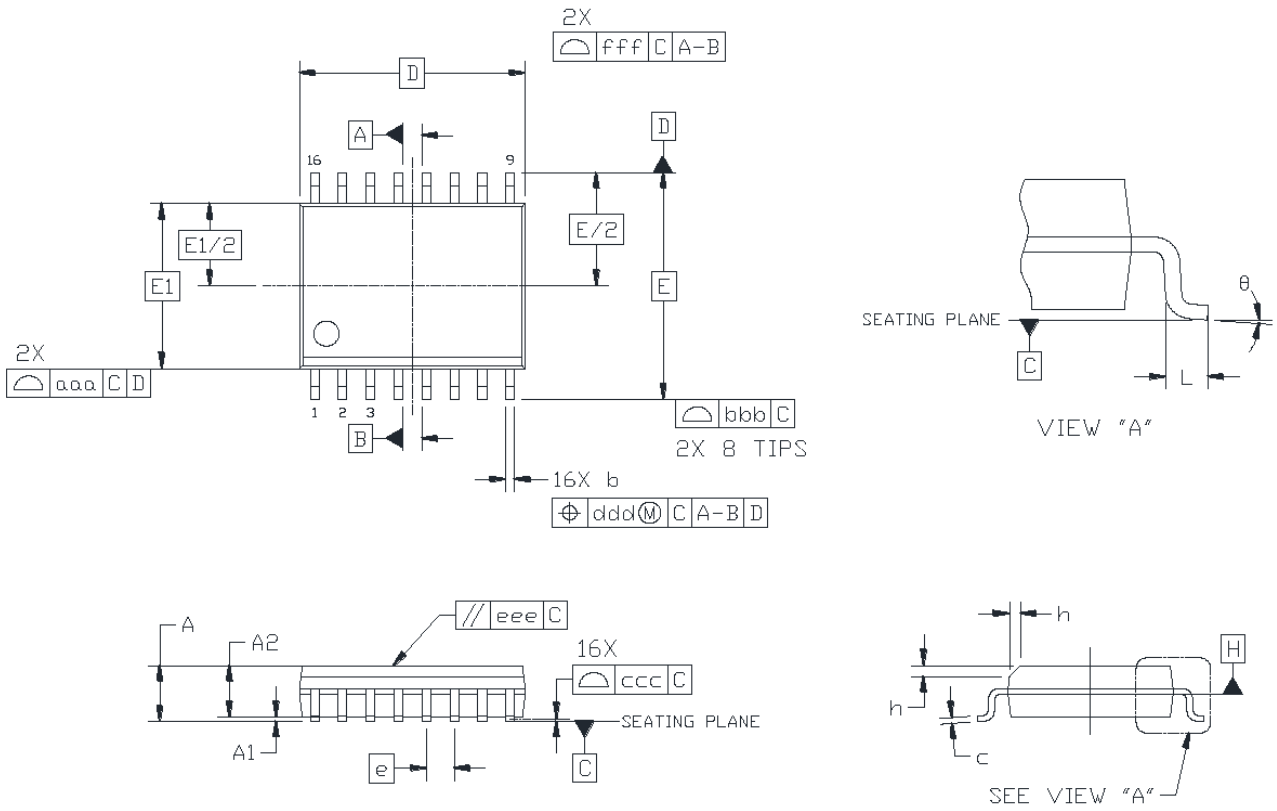


Figure 7.1. 16 引脚宽体 SOIC

Table 7.1. Package Diagram Dimensions

Dimension	Min	Max
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	10.30 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75

Dimension	Min	Max
θ	0°	8°
α α α	—	0.10
bbb	—	0.33
ccc	—	0.10
ddd	—	0.25
eee	—	0.10
fff	—	0.20

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AA.
4. Recommended reflow profile per JEDEC J-STD-020 specification for small body, lead-free components.

7.2 封装外形：16 引脚窄体 SOIC

Figure 7.2 16 引脚小外形集成电路 (SOIC) 封装 on page 42 给出了 16 引脚窄体 SOIC (SO-16) 中 Si823x 的封装细节。Table 7.2 Package Diagram Dimensions on page 42 列出了图示中尺寸的值。

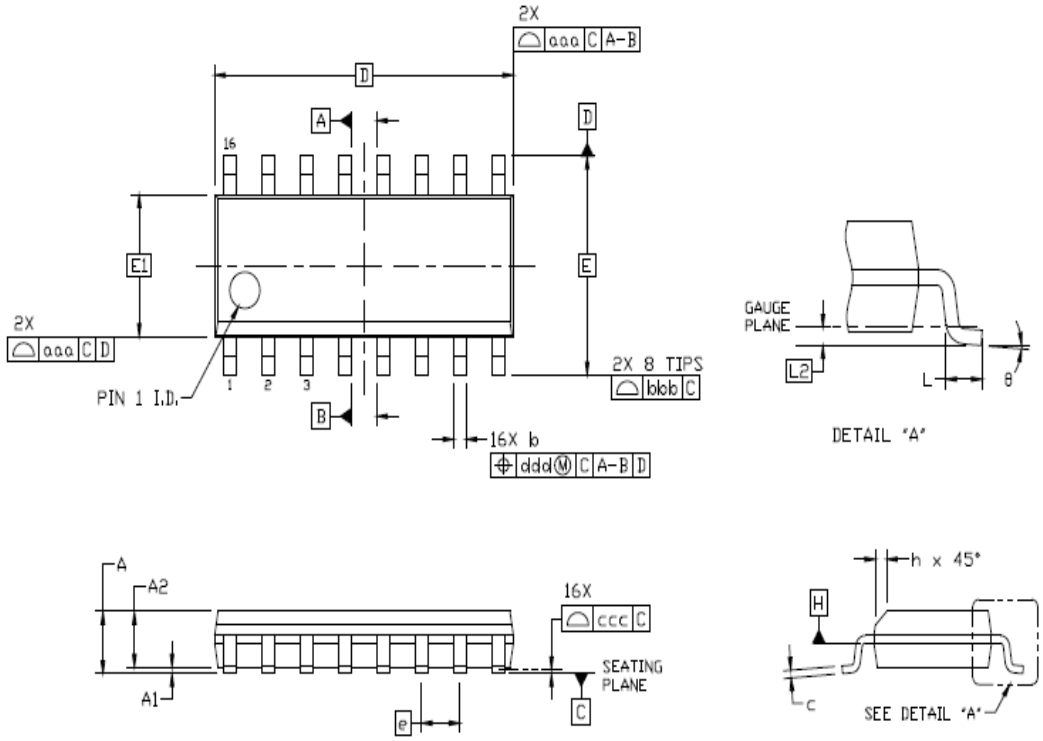


Figure 7.2. 16 引脚小外形集成电路 (SOIC) 封装

Table 7.2. Package Diagram Dimensions

Dimension	Min	Max		Dimension	Min	Max
A	—	1.75		L	0.40	1.27
A1	0.10	0.25		L2	0.25 BSC	
A2	1.25	—		h	0.25	0.50
b	0.31	0.51		θ	0°	8°
c	0.17	0.25		aaa	0.10	
D	9.90 BSC			bbb	0.20	
E	6.00 BSC			ccc	0.10	
E1	3.90 BSC			ddd	0.25	
e	1.27 BSC					

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.3 封装外形：14 LD LGA (5 x 5 mm)

Figure 7.3 Si823x LGA 外形 on page 43 给出了 LGA 外形下 Si823x 的封装细节。Table 7.3 Package Diagram Dimensions on page 43 列出了图示中尺寸的值。

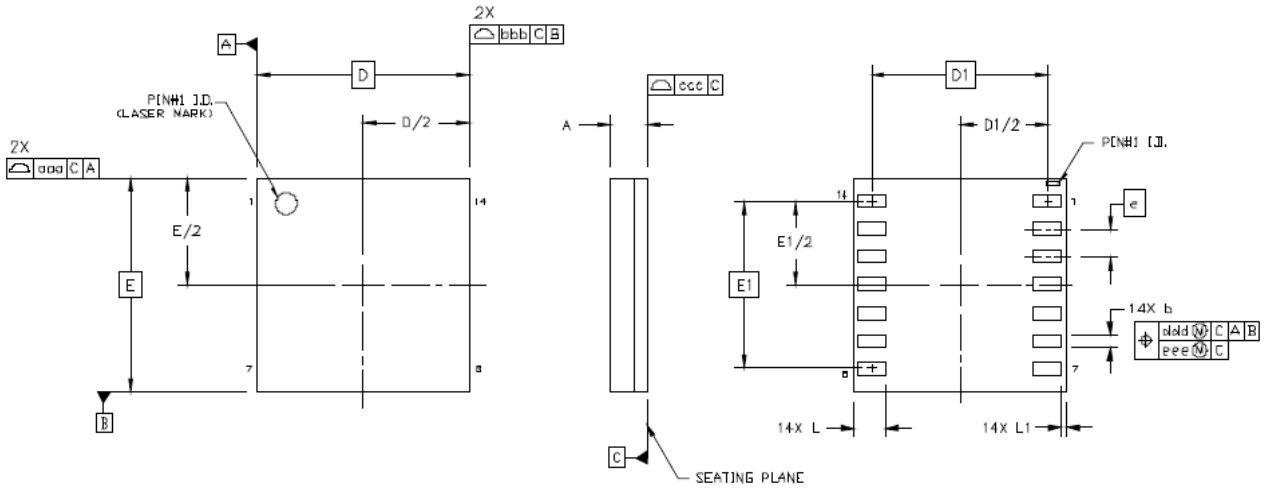


Figure 7.3. Si823x LGA 外形

Table 7.3. Package Diagram Dimensions

Dimension	MIN	NOM	MAX
A	0.74	0.84	0.94
b	0.25	0.30	0.35
D		5.00 BSC	
D1		4.15 BSC	
e		0.65 BSC	
E		5.00 BSC	
E1		3.90 BSC	
L	0.70	0.75	0.80
L1	0.05	0.10	0.15
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.15
eee	—	—	0.08

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

7.4 封装外形：14 LD LGA 及导热垫 (5 x 5 mm)

Figure 7.4 Si823x LGA 及导热垫外形 on page 44 给出了 LGA 外形下 Si8236 ISOdriver 的封装细节。Table 7.4 Package Diagram Dimensions on page 44 列出了图示中尺寸的值。

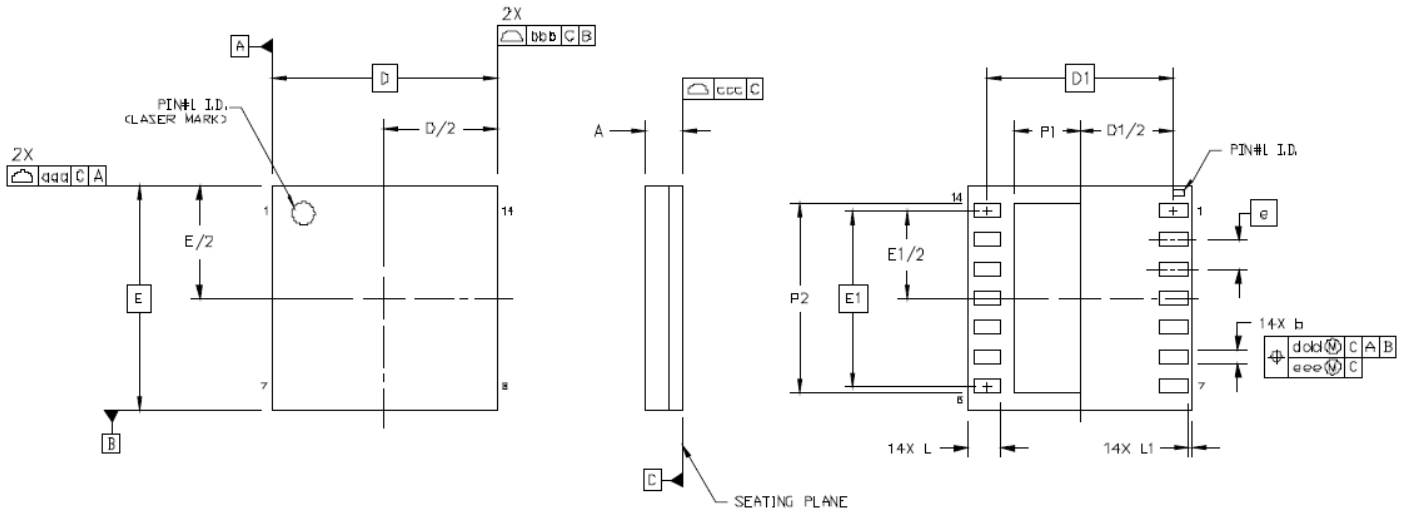


Figure 7.4. Si823x LGA 及导热垫外形

Table 7.4. Package Diagram Dimensions

Dimension	MIN	NOM	MAX
A	0.74	0.84	0.94
b	0.25	0.30	0.35
D		5.00 BSC	
D1		4.15 BSC	
e		0.65 BSC	
E		5.00 BSC	
E1		3.90 BSC	
L	0.70	0.75	0.80
L1	0.05	0.10	0.15
P1	1.40	1.45	1.50
P2	4.15	4.20	4.25
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.15
eee	—	—	0.08

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

8. 焊盘图案

8.1 焊盘图案：16 引脚宽体 SOIC

Figure 8.1 16 引脚 SOIC 焊盘图案 on page 45 给出了 16 引脚宽体 SOIC 中 Si823x 的建议焊盘详细信息。Table 8.1 16-Pin Wide Body SOIC Land Pattern Dimensions on page 45 列出了图示中尺寸的值。

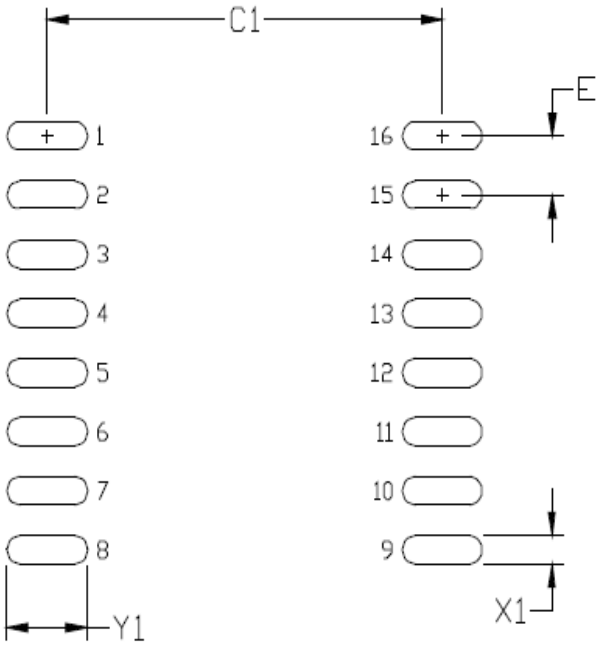


Figure 8.1. 16 引脚 SOIC 焊盘图案

Table 8.1. 16-Pin Wide Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.90

Notes:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

8.2 焊盘图案：16 引脚窄体 SOIC

Figure 8.2 16 引脚窄体 SOIC PCB 焊盘图案 on page 46 说明了 16 引脚窄体 SOIC 中 Si823x 的推荐焊盘图案详细信息。Table 8.2 16-Pin Narrow Body SOIC Land Pattern Dimensions on page 46 列出了图示中尺寸的值。

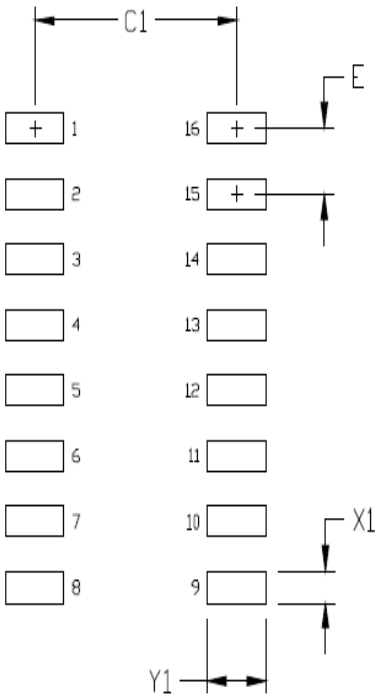


Figure 8.2. 16 引脚窄体 SOIC PCB 焊盘图案

Table 8.2. 16-Pin Narrow Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Notes:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

8.3 焊盘图案：14 LD LGA

Figure 8.3 14 引脚 LGA 焊盘图案 on page 47 说明了 在 14 引脚 LGA 中 Si823x 的推荐焊盘图案详细信息。Table 8.3 14-Pin LGA Land Pattern Dimensions on page 47 列出了图示中尺寸的值。

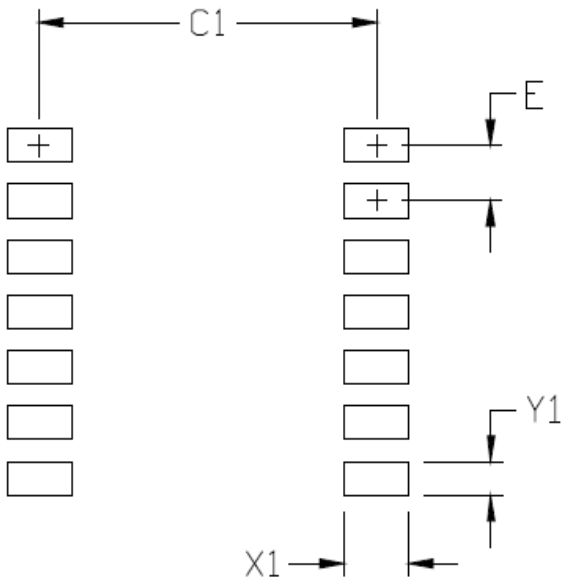


Figure 8.3. 14 引脚 LGA 焊盘图案

Table 8.3. 14-Pin LGA Land Pattern Dimensions

Dimension	(mm)
C1	4.20
E	0.65
X1	0.80
Y1	0.40

Notes:

General

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.4 焊盘图案：14 LD LGA 及导热垫

Figure 8.4 14 引脚 LGA 及导热垫焊盘图案 on page 48 说明了 14 引脚 LGA 及导热垫中 Si8236 的推荐焊盘图案详细信息。Table 8.4 14-Pin LGA with Thermal Pad Land Pattern Dimensions on page 48 列出图中尺寸值。

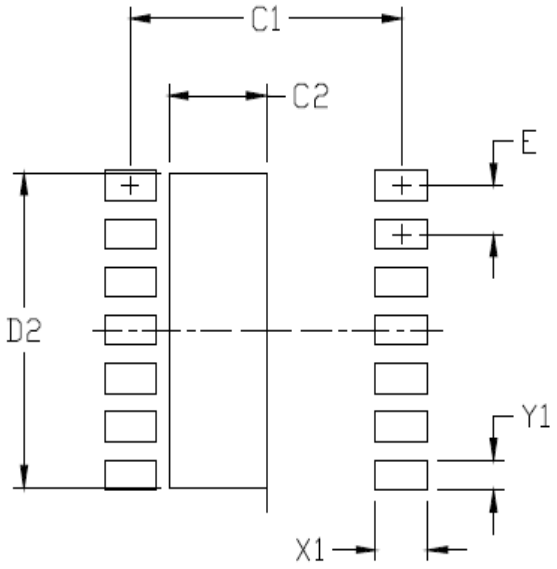


Figure 8.4. 14 引脚 LGA 及导热垫焊盘图案

Table 8.4. 14-Pin LGA with Thermal Pad Land Pattern Dimensions

Dimension	(mm)
C1	4.20
C2	1.50
D2	4.25
E	0.65
X1	0.80
Y1	0.40

Dimension	(mm)

Notes:

General

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. 顶部标记

9.1 Si823x 顶部标记（16 引脚宽体 SOIC）

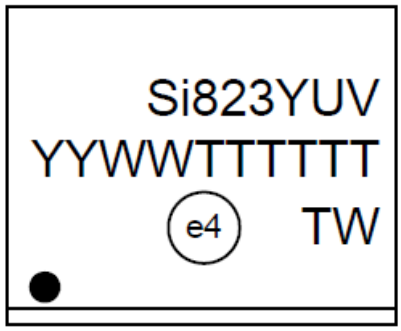
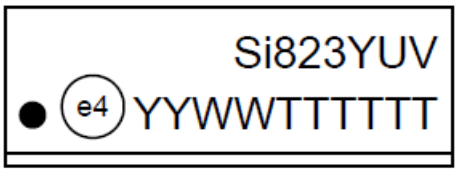


Table 9.1. Top Marking Explanation (16-Pin Wide Body SOIC)

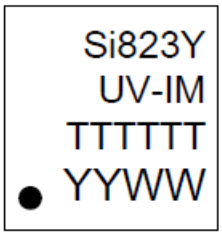
Line 1 Marking:	Base Part Number Ordering Options See Ordering Guide for more information.	Si823 = ISOdriver product series Y = Peak output current 0, 1, 2, 7 = 0.5 A 3, 4, 5, 8 = 4.0 A U = UVLO level A = 5 V; B = 8 V; C = 10 V; D = 12.5 V V = Isolation rating B = 2.5 kV; C = 3.75 kV; D = 5.0 kV
Line 2 Marking:	YY = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the year and workweek of the mold date.
	TTTTTT = Mfg Code	Manufacturing Code from Assembly Purchase Order form.
Line 3 Marking:	Circle = 1.5 mm Diameter (Center Justified)	“e4” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	TW = Taiwan

9.2 Si823x 顶部标记（16 引脚窄体 SOIC）



Line 1 Marking:	Base Part Number Ordering Options See Ordering Guide for more information.	Si823 = ISOdriver product series Y = Peak output current • 0, 1, 2, 7 = 0.5 A • 3, 4, 5, 8 = 4.0 A U = UVLO level • A = 5 V; B = 8 V; C = 10 V; D = 12.5 V V = Isolation rating • B = 2.5 kV; C = 3.75 kV; D = 5.0 kV
Line 2 Marking:	YY = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the year and workweek of the mold date.
	TTTTTT = Mfg Code	Manufacturing Code from Assembly Purchase Order form.

9.3 Si823x 顶部标记（14 LD LGA）



Line 1 Marking:	Base Part Number Ordering Options See Ordering Guide for more information.	Si823 = ISOdriver product series Y = Peak output current • 0, 1, 2 = 0.5 A • 3, 4, 5, 6 = 4.0 A
Line 2 Marking:	Ordering options	U = UVLO level • A = 5 V; B = 8 V; C = 10 V; D = 12.5 V V = Isolation rating • A = 1.0 kV; B = 2.5 kV; C = 3.75 kV; D = 5.0 kV I = –40 to +125 °C ambient temperature range M = LGA package type
Line 3 Marking:	TTTTTT	Manufacturing Code from Assembly
Line 4 Marking:	Circle = 1.5 mm diameter	Pin 1 identifier
	YYWW	Manufacturing date code

10. 版本历史

10.1 修订版 0.11

- 首次发行。

10.2 版本 0.2

- 更新了所有规格以反映最新修订。
- 更新的 Table 4.1 Electrical Characteristics[1] on page 21，包括新 UVLO 选项。
- 更新的 Table 4.8 Absolute Maximum Ratings[1] on page 28，反映新的最大封装隔离额定值
- 添加了图 34、35 和 36。
- 更新了订购指南以反映新封装选项。
- 添加了“欠压锁定 (UVLO)”章节以描述 UVLO 操作。

10.3 版本 0.3

- 第 2、3 和 4 章移动到了第 5 章之后。
- 更新了表格 Table 6.4 Si8233 Two-Input HS/LS Isolated Driver (14 LD LGA) on page 36、Table 6.5 Si8234 PWM Input HS/LS Isolated Driver (14 LD LGA) on page 37 和 Table 6.7 Si8236 Dual Isolated Driver (14 LD LGA) on page 39。
  - 从引脚图和标题中删除 Si8230、Si8231 和 Si8232。
- 更新和添加了订购指南脚注。
- 更新了 Table 4.1 Electrical Characteristics[1] on page 21 中的 UVLO 规格。
- 在 Table 4.1 Electrical Characteristics[1] on page 21 中增加了 PWD 和输出供电有效电流规格。
- 在 3.3 典型工作特征（0.5 安培） 和 3.4 典型工作特征（4.0 安培）中更新和增加了典型工作条件图。

10.4 版本 1.0

- 已更新表 Table 4.2 Regulatory Information[1, 2, 3, 4] on page 25、Table 4.3 Insulation and Safety-Related Specifications on page 26、Table 4.4 IEC 60664-1 (VDE 0884 Part 5) Ratings on page 26 和 Table 4.5 IEC 60747-5-5 Insulation Characteristics[1] on page 27。
- 更新了 2. 订购指南。
  - 添加了 5 V UVLO 订购选项
- 添加了标记部分。

10.5 版本 1.1

- 更新了 1. 功能列表。
  - CMTI 规格更新。
- 更新了 Table 4.1 Electrical Characteristics[1] on page 21。
  - CMTI 规格更新。
- 更新了 Table 4.5 IEC 60747-5-5 Insulation Characteristics[1] on page 27。
- 更新了 5.2 双驱动器。
- 更新了 2. 订购指南。
- 第 1 页上使用芯片图形替代引脚说明。

10.6 版本 1.2

- 更新了 2. 订购指南。
  - 更新了所有封装类型的湿敏度 (MSL)。
- 更新了 Table 4.8 Absolute Maximum Ratings[1] on page 28。
  - 添加了结点温度规格。
- 已更新 Table 4.2 Regulatory Information[1, 2, 3, 4] on page 25，带新的注释。
- 添加了表格 Table 6.7 Si8236 Dual Isolated Driver (14 LD LGA) on page 39 和引出线。
- 更新的图 Figure 3.16 相对于供电电压的输出吸入电流 on page 9、Figure 3.14 相对于供电电压的输出源电流 on page 9、Figure 3.17 相对于温度的输出吸入电流 on page 9 和 Figure 3.15 相对于温度的输出源电流 on page 9，说明正确的 y 轴比例。
- 更新了 Figure 5.2 双驱动器应用中的 Si8232/5/7/8 on page 32。
- 更新了 5.3 双驱动器及热增强封装 (Si8236)。
- 更新了 7.1 封装外形：16 引脚宽体 SOIC。
- 更新了 Table 7.1 Package Diagram Dimensions on page 40。
- 将提到的 1.5 kV_{RMS} 额定器件全部改为 1.0 kV_{RMS}。
- 更新了 3.7 功率耗散考虑。

10.7 修订版 1.3

- 全文添加了 Si8237/8。
- 更新了 Table 4.1 Electrical Characteristics[1] on page 21。
- 更新了 Figure 4.1 IOL 吸收电流测试电路 on page 24。
- 更新了 Figure 4.2 IOH 源电流测试电路 on page 24。
- 增加了 Figure 4.3 共模瞬态抗扰度测试电路 on page 25。
- 更新了 Si823x 产品系列真值表以包括注释 1 和 2。
- 更新了 3.10 可编程死区时间和重叠保护。
- 删除了图 26A 和 26B 的参考。
- 更新了 Table 2.1 Si823x Ordering Guide [1, 2] on page 2。
- 添加了 Si8235-BA-C-IS1 订购部件号。
- 添加了表的注意。

10.8 修订版 1.4

- 更新了 2. 订购指南。
  - 更新了"3 V VDDI 订购选项"。

10.9 修订版 1.5

- 更新了 Table 4.1 Electrical Characteristics[1] on page 21，输入、输出供电电流。
- 全文增加了对 AEC-Q100 认证的引用。
- 将所有对 60747-5-2 的引用更改为 60747-5-5。
- 全文增加了对 CQC 的引用。
- 全面更新了引脚说明。
  - 将死区时间默认值从 1 ns 更正为 400 ps。
- 更新了 Table 2.1 Si823x Ordering Guide [1, 2] on page 2 中的“订购部件号”。
  - 删除了湿敏度表格注释。

10.10 修订版 1.6

- 更新了 Table 2.1 Si823x Ordering Guide [1, 2] on page 2，订购零件号。
- 增加了修订版 D 订购零件号。
- 删除了之前修订版本的所有订购零件号。

10.11 修订版 1.7

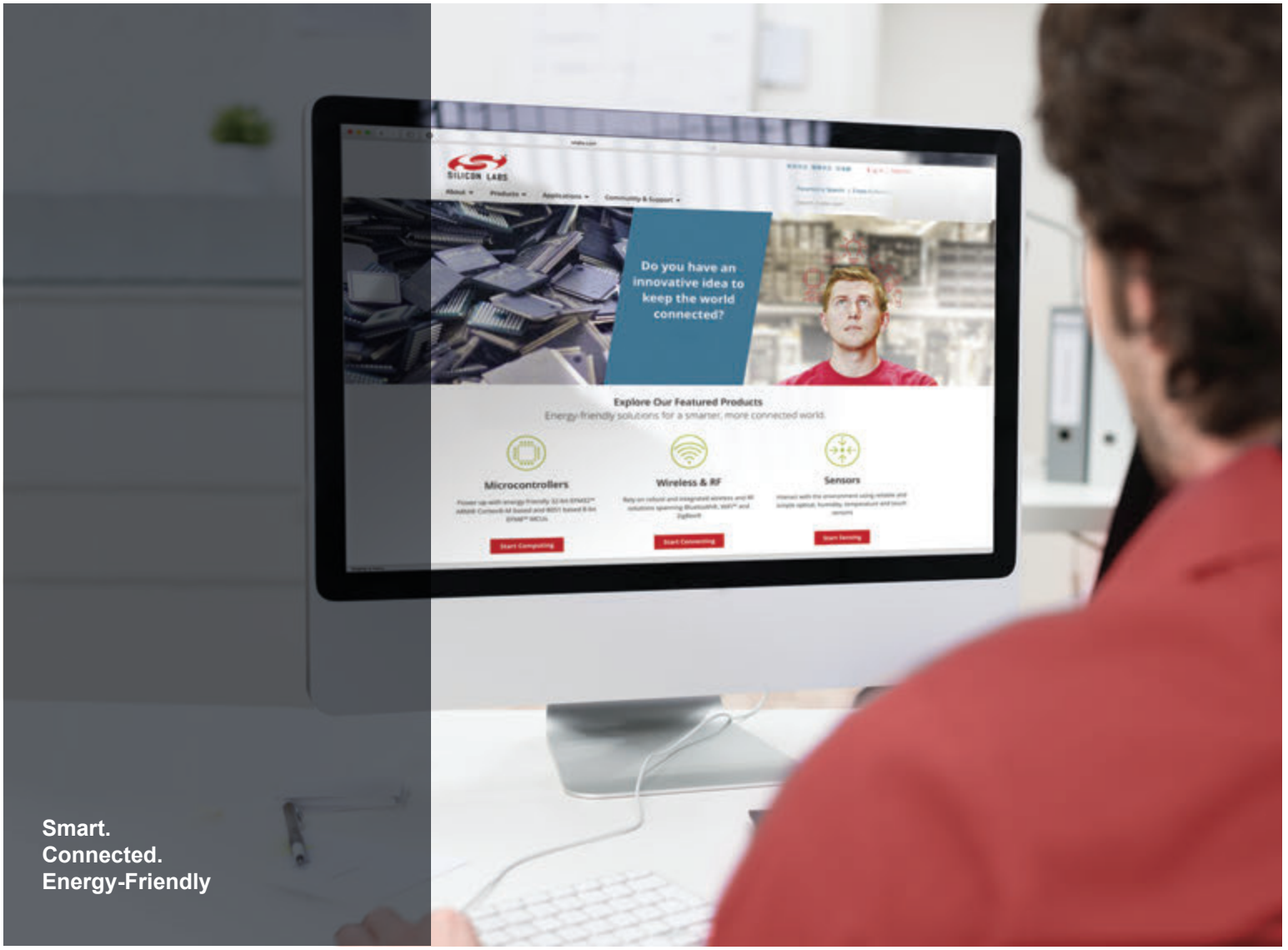
- 更新了 Table 4.2 Regulatory Information[1, 2, 3, 4] on page 25
  - 添加了合规认证（CQC）号码。
- 更新了 Table 4.3 Insulation and Safety-Related Specifications on page 26
  - 更新了侵蚀深度。
- 更新了 Table 4.5 IEC 60747-5-5 Insulation Characteristics[1] on page 27
  - 更新了 WBSOIC-16 的 V_{PR}。
- 更新了 Table 4.8 Absolute Maximum Ratings[1] on page 28
  - 删除了 Io，添加了峰值输出电流规格。
- 更新了公式 1。
- 更新了Figure 5.1 半桥应用中的 Si823x on page 31。
- 更新了Figure 5.2 双驱动器应用中的 Si8232/5/7/8 on page 32。
- 更新了“订购指南”Table 2.1 Si823x Ordering Guide [1, 2] on page 2。
  - 删除了注释 2。

10.12 修订版 1.8

2016 年 5 月 17 日

- 将文档从 Framemaker 转换为 DITA。

目录



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