EFM32 Giant Gecko Series 1 家庭 EFM32GG11 产品系列数据表

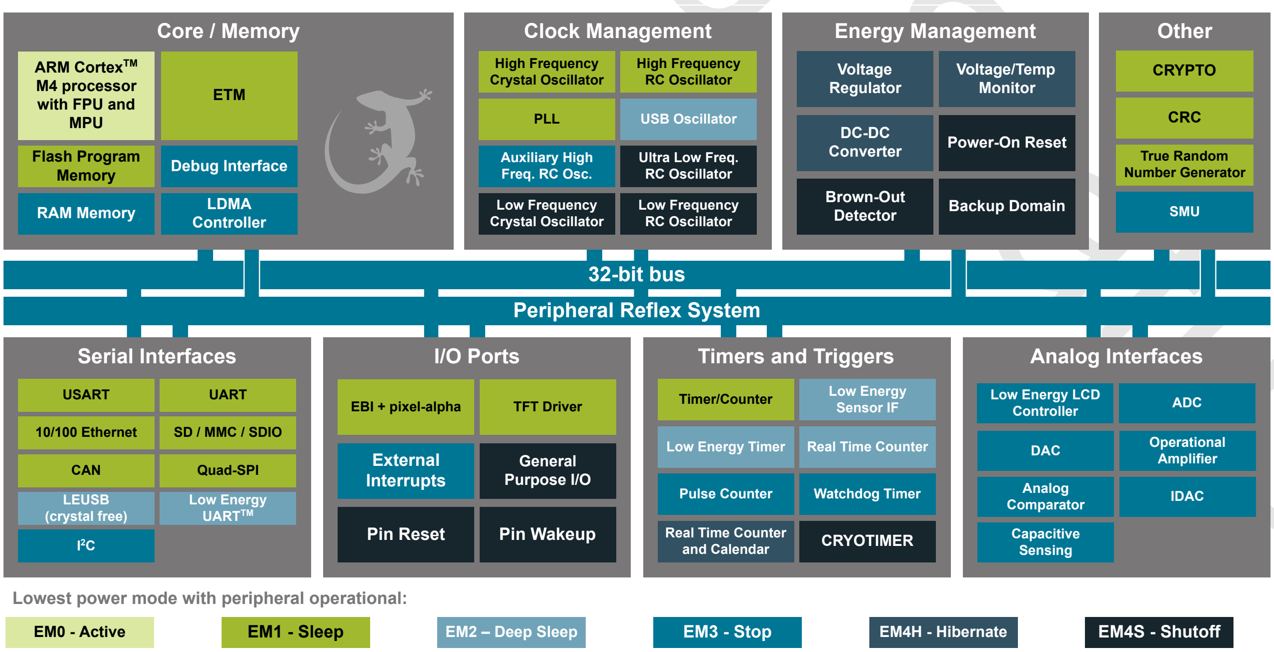
EFM32 Giant Gecko 系列 1 MCU 是世界上最节能的微控制器，具有新型连接接口和用户界面功能。

EFM32GG11 配有强大的 32 位 ARM® Cortex®-M4，并可通过支持 AES、ECC、SHA 和真随机数生成器 (TRNG) 的独特加密硬件引擎，提供强化安全。新功能包括 SD/MMC/SDIO 控制器、Octal/Quad-SPI 存储控制器、10/100 以太网媒体接入控制器、控制器局域网控制器、高度增强的电容式感应、极速图形引擎（alpha 混合）以及 LESENSE/PCNT 智能电能表增强功能。这些功能结合超低电流活动模式，再加上从节能模式快速唤醒功能，使得 EFM32GG11 微控制器既适用于任何电池供电的应用，也适合有着高性能和低能耗要求的其他系统。

示例应用程序：

- 智能电能表
- 工业和工厂自动化
- 家庭自动化和安全
- 中级和高级可穿戴设备
- 物联网设备

- ARM Cortex-M4（功率为 72 MHz）
- 超低能耗操作
  - 能量模式 0（EM0）为 77 µA/MHz
  - 在 EM2 深度睡眠模式下，电流为 1.6 µA（RTCC 运行，状态/RAM 保留）
- Octal/Quad-SPI 存储控制器接口（支持芯片内执行）
- SD/MMC/SDIO 主机控制器
- 10/100 以太网媒体接入控制器，符合 802.3az EEE、IEEE1588 节能规范
- 控制器局域网 2.0 双控制器
- 无晶体低能耗 USB
- 支持 AES、ECC、SHA 和 TRNG 的硬件加密引擎
- 增强的电容式触摸感应
- 与特定 EFM32 封装兼容
- 5 V 容差 I/O



1. 功能列表

EFM32GG11 重要功能如下所列。

- **ARM Cortex-M4 CPU 平台**
  - High performance 32-bit processor @ up to 72 MHz
  - DSP instruction support and Floating Point Unit
  - Memory Protection Unit
  - Wake-up Interrupt Controller
- **灵活能源管理系统**
  - 在活动模式下（EM0），功耗为 77 μA/MHz
  - 在 EM2 深度睡眠模式下，电流为 1.6 μA（16 kB RAM 保留，从 LFRCO 运行 RTCC）
- **集成直流到直流降压转换器**
- **高达 2048 kB 的闪存程序存储器**
  - 双组闪存，支持读写同步
- **高达 512 kB 的 RAM 数据存储**
  - 256 kB 纠错内存（SEC-DED 汉明码）
- **Octal/Quad-SPI 闪存存储接口**
  - 支持 3 V 和 1.8 V 内存
  - 1/2/4/8 位数据总线
  - Quad-SPI 芯片内执行（XIP）
  - 3 V 时，SDR 高达 30 MHz，DDR 高达 15 MHz
- **通信接口**
  - 低能耗通用串行总线（USB），可提供设备和主机支持
    - 与 USB 2.0 完全兼容
    - 片上物理层和 5V 至 3.3 V 嵌入式稳压器
    - 无晶体设备模式操作
    - 专利申请中的低能耗模式（LEM）
  - SD/MMC/SDIO 主机控制器
    - SD v3.01、SDIO v3.0 和 MMC v4.51 高达 50 MHz
    - 1/4/8 位总线宽度
  - 10/100 以太网媒体接入控制器，带有 MII/RMII 接口
    - IEEE1588-2008 精密时间戳协议
    - 节能以太网（802.3az）
  - 最多 2 个控制器局域网控制器
    - 2.0A 和 2.0B 版本速度高达 1 Mbps
  - 6 个通用同步/异步接收器/传输器
    - UART/SPI/SmartCard（ISO 7816)/IrDA/I2S/LIN
    - 三重缓冲全双工/半双工操作，带有流控制
    - 在一个实例上的超高速操作（36 MHz）
  - 2 个通用异步接收器/传输器
  - 2 个低能耗 UART
    - 在深度睡眠模式下，使用 DMA 进行自主操作
  - 3 个 I^2C 接口（受 SMBus 支持）
    - EM3 停止模式下的地址识别
- **通用 I/O 引脚最高为 144**
  - 可配置的推挽、开漏、上拉/下拉、输入滤波器和驱动强度
  - 可配置的外围设备 I/O 位置
  - 特定引脚上的 5 V 电压耐受
  - 异步外部中断
  - 输出状态保留和从关机模式唤醒
- **多达 24 个信道 DMA 控制器**
- **用于在外围设备之间自主传输信号的最多 24 个信道外围设备反射系统（PRS）**
- **外部总线接口，适用于最大为 4x256 MB 外部存储器映射空间**
  - 带有直接驱动功能的 TFT 控制器
  - alpha 混合像素引擎
- **硬件加密**
  - AES 128/256 位密匙
  - ECC B/K163、B/K233、P192、P224、P256
  - SHA-1 和 SHA-2（SHA-224 and SHA-256）
  - 真随机数生成器（TRNG）
- **硬件 CRC 引擎**
  - 单周期计算，8/16/32 位数据和 16 位（可编程）/32 位（固定）多项式
- **安全管理单元（SMU）**
  - 为片上外围设备提供细粒度访问控制
- **集成低能耗 LCD 控制器，最多带有 8×36 个分段**
  - 升压、对比度和自主动画
  - 已获专利的低能耗 LCD 驱动器
- **备用电源域**
  - 在单独电源域中的 RTCC 和保留寄存器，适用于能源模式 EM4H
  - 当无主电源或主电源不足时，可使用备用电池进行操作
- **超低功耗精准模拟外围设备**
  - 2 个 12 位 1 M 样本/秒的数字模拟转换器（VDAC）
    - 片上温度传感器
  - 2 个 12 位 500 K 样本/秒的数字模拟转换器（VDAC）
  - 数字模拟电流转换器（IDAC）
  - 多达 4 个模拟比较器（ACMP）
  - 多达 4 个运行放大器（OPAMP）
  - 增强的基于电流的电容式感应，带有多达 64 个输入和触摸唤醒功能（CSEN）
  - 多达 108 个具有模拟功能的 GPIO 引脚。使用模拟端口（APORT）的灵活模拟外设引脚路由
  - 电源电压监控器

- **定时器/计数器**
  - 7 个 16 位定时器/计数器
    - 3+4 个对比/捕捉/PWM 通道（4+4 个位于一个定时器实例）
    - 多个定时器实例上插入失效时间
  - 4 个 32 位计数器/定时器
  - 32 位实时计数器和日历 (RTCC)
  - 24 位实时计数器 (RTC)
  - 可从任何能耗模式定期唤醒的 32 位超低能耗 CRYOTIMER
  - 2 个用于波形生成的 16 位低能耗定时器
  - 3 个带有异步操作的 16 位脉冲计数器
  - 2 个带有专用 RC 振荡器的监视程序定时器
- **低能耗传感器接口 (LESENSE)**
  - 在深度睡眠模式下进行传感器自主监控
  - 支持多种传感器，包括 LC 传感器和电容式按钮
  - 多达 16 个输入
- **超高效的加电复位和欠压检测器**
- **调试接口**
  - 2 引脚串行线调试接口
  - 1 引脚串行线查看器
  - 4 引脚 JTAG 接口
  - 嵌入式追踪宏单元 (ETM)
- **预编程 USB/UART 引导装载程序**
- **较宽工作范围**
  - 1.8 至 3.8 V 单电源
  - 集成的直流到直流，系统负载电流高达 200 mA 时，输出电压低至 1.8 V
  - 提供标准温度范围（-40 ° C 至 85 ° C T_{AMB}）和更大温度范围（-40 ° C 至 125 ° C T_J）
- **封装**
  - QFN64（9x9 mm）
  - TQFP64（10x10 mm）
  - TQFP100（14x14 mm）
  - BGA112（10x10 mm）
  - BGA120（7x7 mm）
  - BGA152（8x8 mm）
  - BGA192（7x7mm）

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	DC-DC Converter	USB	Ethernet	QSPI	SDIO	LCD	GPIO	Package	Temp Range
EFM32GG11B820F2048GL192-X	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	144	BGA192	-40 to +85
EFM32GG11B820F2048GQ100-X	2048	512	Yes	Yes	Yes	Yes	Yes	Yes	80	QFP100	-40 to +85

Note:

1. Ordering codes ending in -X indicate pre-production engineering status devices. Engineering status devices are provided for development use only. They should not be used for product qualification and are not available in production quantities.

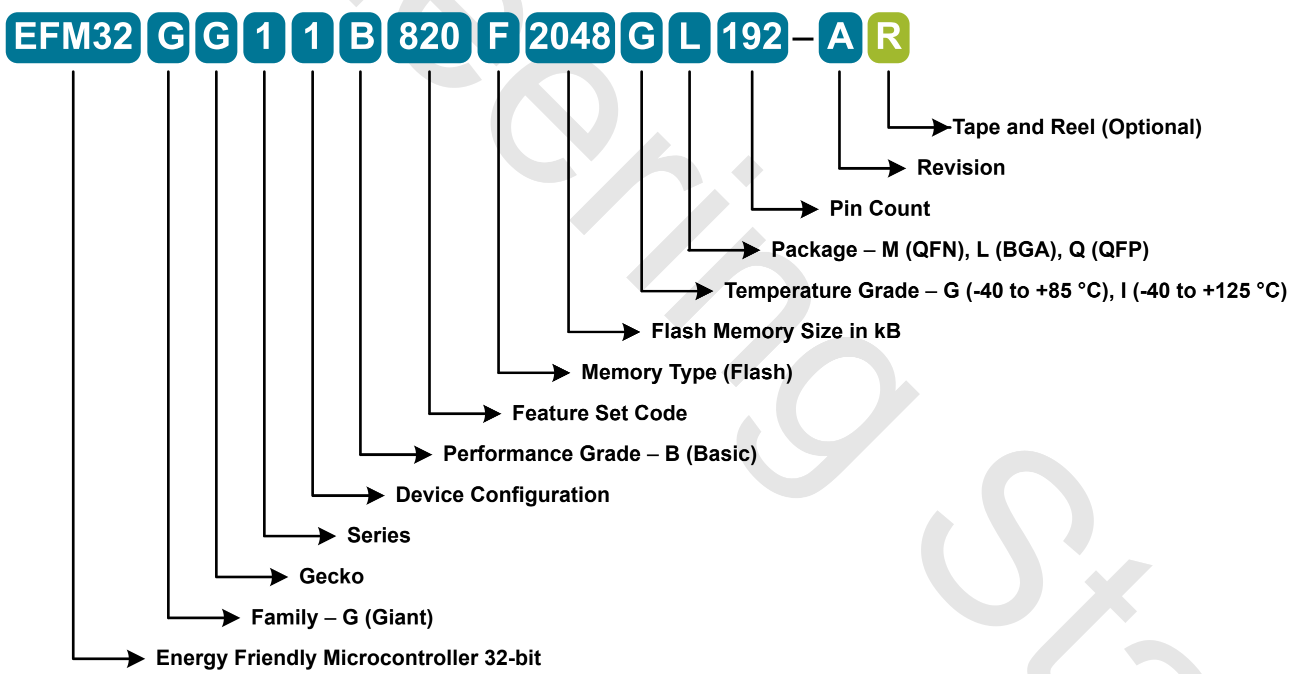


Figure 2.1. OPN Decoder

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3. System Overview

3.1 Introduction

The Giant Gecko Series 1 product family is well suited for any battery operated application as well as other systems requiring high performance and low energy consumption. This section gives a short introduction to the MCU system. The detailed functional description can be found in the Giant Gecko Series 1 Reference Manual.

A block diagram of the Giant Gecko Series 1 family is shown in Figure 3.1 Detailed EFM32GG11 Block Diagram on page 8. The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult Ordering Information.

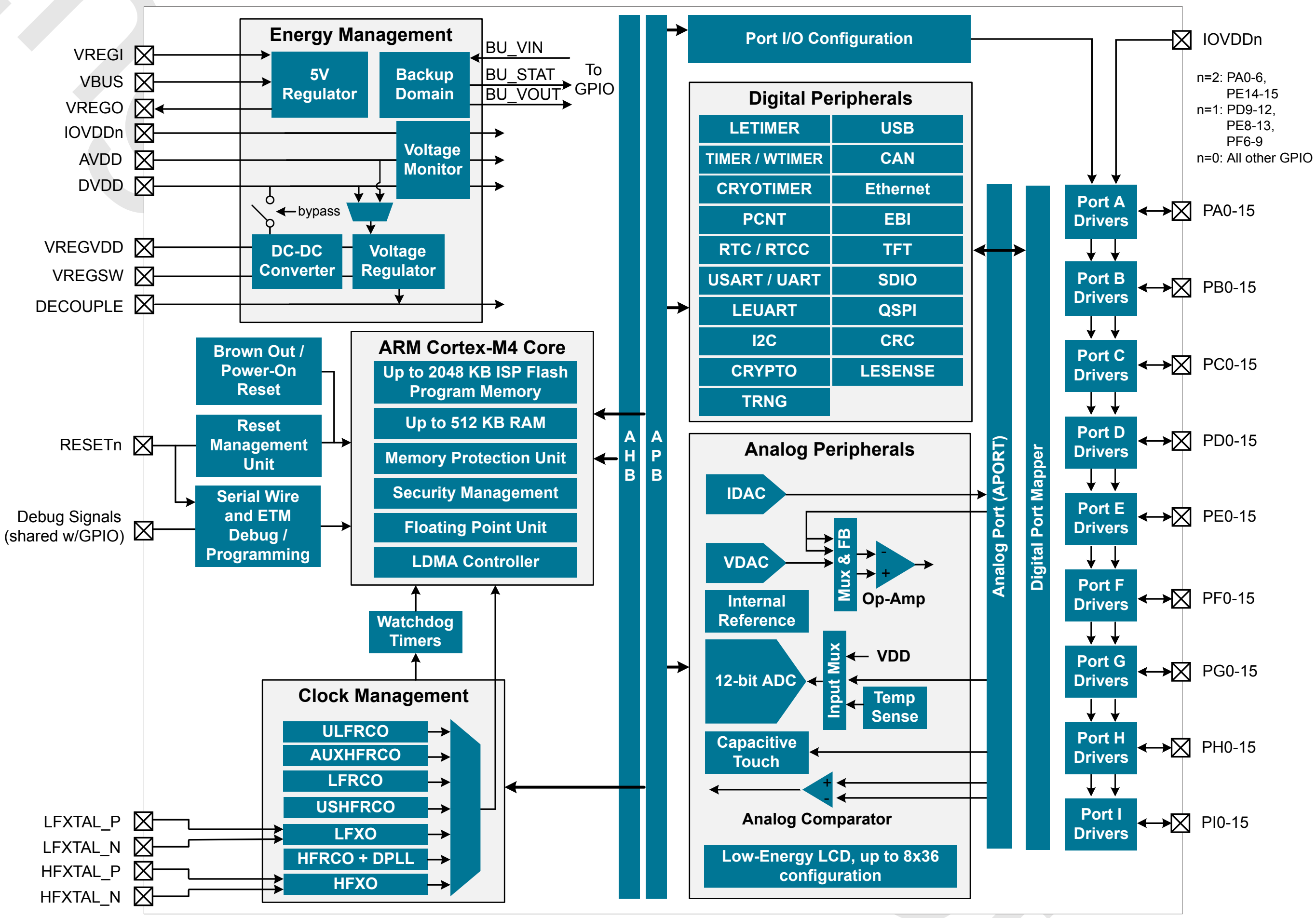


Figure 3.1. Detailed EFM32GG11 Block Diagram

3.2 Power

The EFM32GG11 has an Energy Management Unit (EMU) and efficient integrated regulators to generate internal supply voltages. Only a single external supply voltage is required, from which all internal voltages are created. A 5 V regulator is available on some OPNs, allowing the device to be powered directly from 5 V power sources, such as USB. An optional integrated DC-DC buck regulator can be utilized to further reduce the current consumption. The DC-DC regulator requires one external inductor and one external capacitor.

The EFM32GG11 device family includes support for internal supply voltage scaling, as well as two different power domain groups for peripherals. These enhancements allow for further supply current reductions and lower overall power consumption.

AVDD and VREGVDD need to be 1.8 V or higher for the MCU to operate across all conditions; however the rest of the system will operate down to 1.62 V, including the digital supply and I/O. This means that the device is fully compatible with 1.8 V components. Running from a sufficiently high supply, the device can use the DC-DC to regulate voltage not only for itself, but also for other PCB components, supplying up to a total of 200 mA.

3.2.1 Energy Management Unit (EMU)

The Energy Management Unit manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to turn off the power to unused RAM blocks, and it contains control registers for the DC-DC regulator and the Voltage Monitor (VMON). The VMON is used to monitor multiple supply voltages. It has multiple channels which can be programmed individually by the user to determine if a sensed supply has fallen below a chosen threshold.

3.2.2 DC-DC Converter

The DC-DC buck converter covers a wide range of load currents and provides up to 90% efficiency in energy modes EM0, EM1, EM2 and EM3, and can supply up to 200 mA to the device and surrounding PCB components. Protection features include programmable current limiting, short-circuit protection, and dead-time protection. The DC-DC converter may also enter bypass mode when the input voltage is too low for efficient operation. In bypass mode, the DC-DC input supply is internally connected directly to its output through a low resistance switch. Bypass mode also supports in-rush current limiting to prevent input supply voltage droops due to excessive output current transients.

3.2.3 5 V Regulator

A 5 V input regulator is available, allowing the device to be powered directly from 5 V power sources such as the USB VBUS line. The regulator is available in all energy modes, and outputs 3.3 V to be used to power the USB PHY and other 3.3 V systems. Two inputs to the regulator allow for seamless switching between local and external power sources.

3.2.4 EM2 and EM3 Power Domains

The EFM32GG11 has three independent peripheral power domains for use in EM2 and EM3. Two of these domains are dynamic and can be shut down to save energy. Peripherals associated with the two dynamic power domains are listed in Table 3.1 EM2 and EM3 Peripheral Power Subdomains on page 10. If all of the peripherals in a peripheral power domain are unused, the power domain for that group will be powered off in EM2 and EM3, reducing the overall current consumption of the device. Other EM2, EM3, and EM4-capable peripherals and functions not listed in the table below reside on the primary power domain, which is always on in EM2 and EM3.

Table 3.1. EM2 and EM3 Peripheral Power Subdomains

Peripheral Power Domain 1	Peripheral Power Domain 2
ACMP0	ACMP1
PCNT0	PCNT1
ADC0	PCNT2
LETIMER0	CSEN
LESENSE	VDAC0
APORT	LEUART0
-	LEUART1
-	LETIMER1
-	I2C0
-	I2C1
-	I2C2
-	IDAC
-	ADC1
-	ACMP2
-	ACMP3
-	LCD
-	RTC

3.3 General Purpose Input/Output (GPIO)

EFM32GG11 has up to 144 General Purpose Input/Output pins. GPIO are organized on three independent supply rails, allowing for interface to multiple logic levels in the system simultaneously. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

3.4 Clocking

3.4.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFM32GG11. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.4.2 Internal and External Oscillators

The EFM32GG11 supports two crystal oscillators and fully integrates five RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU. Crystal frequencies in the range from 4 to 50 MHz are supported. An external clock source such as a TCXO can also be applied to the HFXO input for improved accuracy over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system. The HFRCO employs fast startup at minimal energy consumption combined with a wide frequency range. When crystal accuracy is not required, it can be operated in free-running mode at a number of factory-calibrated frequencies. A digital phase-locked loop (DPLL) feature allows the HFRCO to achieve higher accuracy and stability by referencing other available clock sources such as LFXO and HFXO.
- An integrated auxilliary high frequency RC oscillator (AUXHFRCO) is available for timing the general-purpose ADC and the Serial Wire Viewer port with a wide frequency range.
- An integrated auxilliary high frequency RC oscillator (USHFRCO) is available for timing the USB, SDIO and QSPI peripherals. The USHFRCO can be syncronized to the host's USB clock to allow the USB to operate in device mode without the additional cost of an external crystal.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) can be used as a timing reference in low energy modes, when crystal accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.5 Counters/Timers and PWM

3.5.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each TIMER is a 16-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit TIMER_0 only.

3.5.2 Wide Timer/Counter (WTIMER)

WTIMER peripherals function just as TIMER peripherals, but are 32 bits wide. They keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the PRS system. The core of each WTIMER is a 32-bit counter with up to 4 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the WTIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers, with optional dead-time insertion available in timer unit WTIMER_0 only.

3.5.3 Real Time Counter and Calendar (RTCC)

The Real Time Counter and Calendar (RTCC) is a 32-bit counter providing timekeeping in all energy modes. The RTCC includes a Binary Coded Decimal (BCD) calendar mode for easy time and date keeping. The RTCC can be clocked by any of the on-board oscillators with the exception of the AUXHFRCO, and it is capable of providing system wake-up at user defined instances. The RTCC includes 128 bytes of general purpose data retention, allowing easy and convenient data storage in all energy modes down to EM4H.

3.5.4 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM2 Deep Sleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.5.5 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

3.5.6 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The module may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

3.5.7 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

3.6 Communications and Other Digital Peripherals

3.6.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I^2S

3.6.2 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous Receiver/Transmitter is a subset of the USART module, supporting full duplex asynchronous UART communication with hardware flow control and RS-485.

3.6.3 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™ provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

3.6.4 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I^2C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

3.6.5 External Bus Interface (EBI)

The External Bus Interface provides access to external parallel interface devices. The interface is memory mapped into the address bus of the Cortex-M4. This enables seamless access from software without manually manipulating the I/O settings each time a read or write is performed. The data and address lines are multiplexed in order to reduce the number of pins required to interface to external devices. Timing is adjustable to meet specifications of the external devices. The interface is limited to asynchronous devices.

The EBI contains a TFT controller which can drive a TFT via an RGB interface. The TFT controller supports programmable display and port sizes and offers accurate control of frequency and setup and hold timing. Direct Drive is supported for TFT displays which do not have their own frame buffer. In that case TFT Direct Drive can transfer data from either on-chip memory or from an external memory device to the TFT at low CPU load. Automatic alpha-blending and masking is also supported for transfers through the EBI interface.

3.6.6 Quad-SPI Flash Controller (QSPI)

The QSPI provides access to to a wide range of flash devices with wide I/O busses. The I/O and clocking configuration is flexible and supports many types of devices. Up to 8-bit wide interfaces are supported. The QSPI handles opcodes, status flag polling, and timing configuration automatically.

The external flash memory is mapped directly to internal memory to allow random access to any word in the flash and direct code execution. An integrated instruction cache minimizes latency and allows efficient code execution. Execute in Place (XIP) is supported for devices with this feature.

Large data chunks can be transferred with DMA as efficiently as possible with high throughput and minimimal bus load, utilizing an integrated 1 kB SRAM FIFO.

3.6.7 SDIO Host Controller (SDIO)

The SDIO is an SD3.01 / SDIO3.0 / eMMC4.51-compliant Host Controller interface for transferring data to and from SD/MMC/SDIO devices. The module conforms to the SD Host Controller Standard Specification Version 3.00. The Host Controller handles SDIO/SD/MMC Protocol at the transmission level, packing data, adding cyclic redundancy check (CRC), Start/End bits, and checking for transaction format correctness. The SDIO interface supports up to 100 Mbps in DS mode and SDR mode, up to 200 Mbps in HS mode, and up to 400 Mbps for eMMC in DDR mode.

3.6.8 Universal Serial Bus (USB)

The USB is a full-speed/low-speed USB 2.0 compliant host/device controller. The USB can be used in device and host-only configurations, while a clock recovery mechanism allows crystal-less operation in device mode. The USB block supports both full speed (12 MBit/s) and low speed (1.5 MBit/s) operation. When operating as a device, a special Low Energy Mode ensures the current consumption is optimized, enabling USB communications on a strict power budget. The USB device includes an internal dedicated Descriptor-Based Scatter/Gather DMA and supports up to 6 OUT endpoints and 6 IN endpoints, in addition to endpoint 0. The on-chip PHY includes internal pull-up and pull-down resistors, as well as voltage comparators for monitoring the VBUS voltage and A/B device identification using the ID line.

3.6.9 Ethernet (ETH)

The Ethernet peripheral is compliant with IEEE 802.3-2002 for Ethernet MAC. It supports 802.1AS and IEEE 1588 precision clock synchronization protocol, as well as 802.3az Energy Efficient Ethernet. The ETH supports a wide variety of frame formats and standard operating modes such as MII/RMII. Direct Memory Access (DMA) support makes it possible to transmit and receive large frames at high data rates with minimal CPU overhead. The Ethernet peripheral supports 10 Mbps and 100 Mbps operation, and includes a total of 8 kB of dedicated dual-port RAM FIFO (4 kB for TX and 4 kB for RX).

3.6.10 Controller Area Network (CAN)

The CAN peripheral provides support for communication at up to 1 Mbps over CAN protocol version 2.0 part A and B. It includes 32 message objects with independent identifier masks and retains message RAM in EM2. Automatic retransmittion may be disabled in order to support Time Triggered CAN applications.

3.6.11 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

3.6.12 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface LESENSE^{TM} is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators, ADC, and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable finite state machine which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

3.7 Security Features

3.7.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

3.7.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. Giant Gecko Series 1 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2^m), and SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO module allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

3.7.3 True Random Number Generator (TRNG)

The TRNG module is a non-deterministic random number generator based on a full hardware solution. The TRNG is validated with NIST800-22 and AIS-31 test suites as well as being suitable for FIPS 140-2 certification (for the purposes of cryptographic key generation).

3.7.4 Security Management Unit (SMU)

The Security Management Unit (SMU) allows software to set up fine-grained security for peripheral access, which is not possible in the Memory Protection Unit (MPU). Peripherals may be secured by hardware on an individual basis, such that only priveleged accesses to the peripheral's register interface will be allowed. When an access fault occurs, the SMU reports the specific peripheral involved and can optionally generate an interrupt.

3.8 Analog

3.8.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

3.8.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.8.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

3.8.4 Capacitive Sense (CSEN)

The CSEN module is a dedicated Capacitive Sensing block for implementing touch-sensitive user interface elements such a switches and sliders. The CSEN module uses a charge ramping measurement technique, which provides robust sensing even in adverse conditions including radiated noise and moisture. The module can be configured to take measurements on a single port pin or scan through multiple pins and store results to memory through DMA. Several channels can also be shorted together to measure the combined capacitance or implement wake-on-touch from very low energy modes. Hardware includes a digital accumulator and an averaging filter, as well as digital threshold comparators to reduce software overhead.

3.8.5 Digital to Analog Current Converter (IDAC)

The Digital to Analog Current Converter can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The full-scale current is programmable between 0.05 µA and 64 µA with several ranges consisting of various step sizes.

3.8.6 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksps, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per single-ended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

3.8.7 Operational Amplifiers

The opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas, and are available down to EM3. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC module or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

3.8.8 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD display with up to 8x36 segments. A voltage boost function enables it to provide the LCD display with higher voltage than the supply voltage for the device. A patented charge redistribution driver can reduce the LCD module supply current by up to 40%. In addition, an animation feature can run custom animations on the LCD display without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

3.9 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFM32GG11. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.10 Core and Memory

3.10.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M4 RISC processor with FPU achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- Embedded Trace Macrocell (ETM) for real-time trace and debug
- Up to 2048 kB flash program memory
  - Dual-bank memory with read-while-write support
- Up to 512 kB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire or 4-pin JTAG debug interface

3.10.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block, whereas the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.10.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.11 Memory Map

The EFM32GG11 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

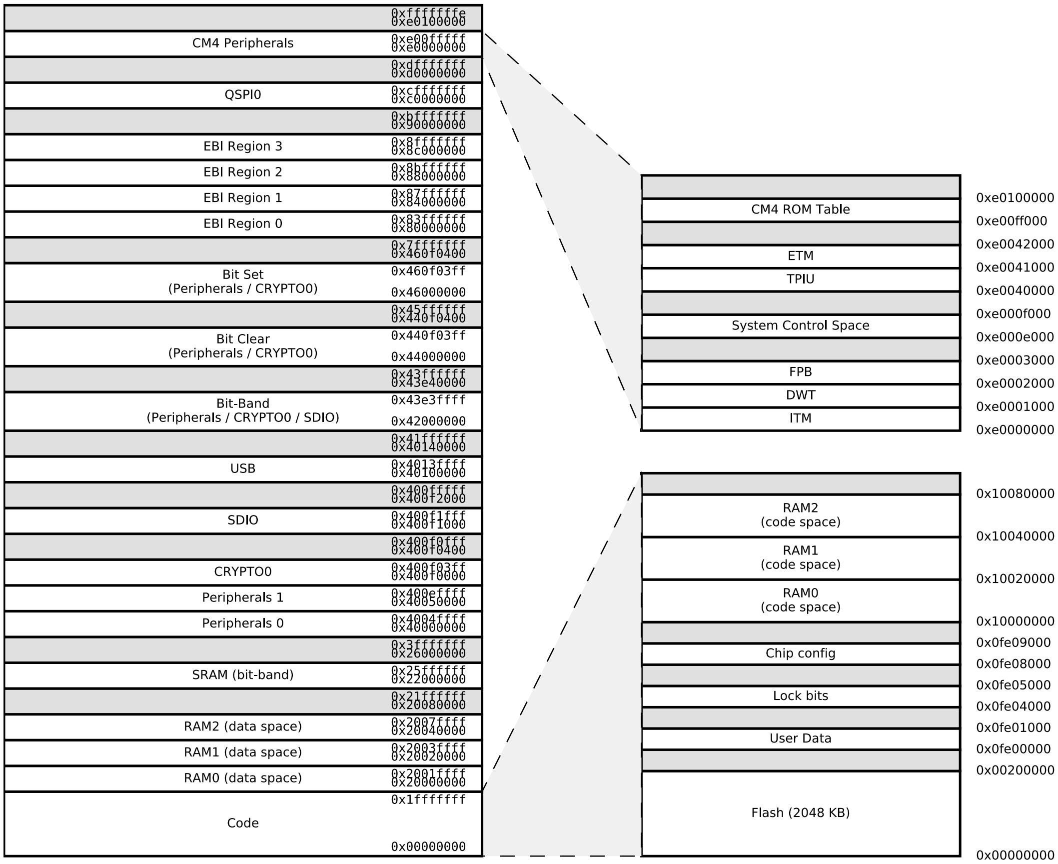


Figure 3.2. EFM32GG11 Memory Map — Core Peripherals and Code Space

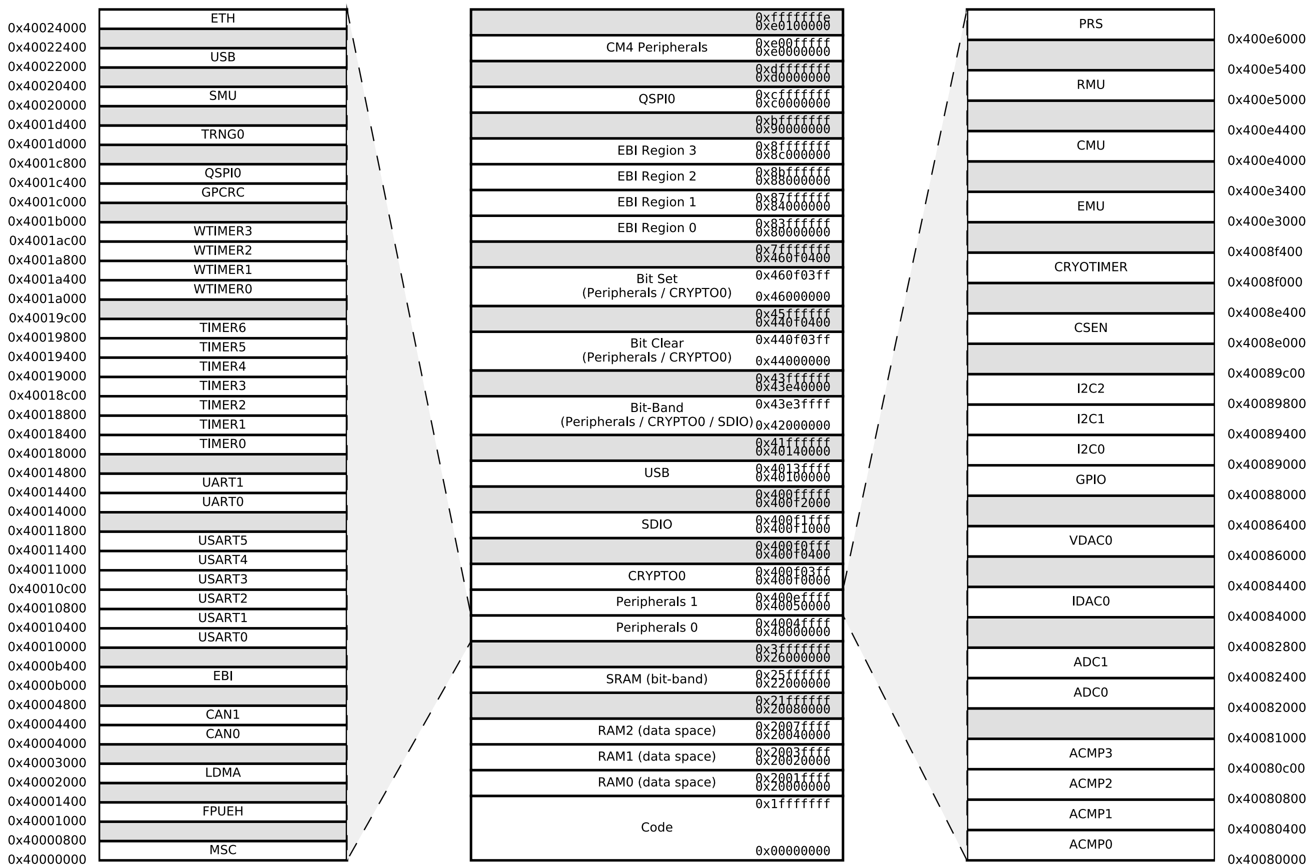


Figure 3.3. EFM32GG11 Memory Map — Peripherals

3.12 Configuration Summary

The features of the EFM32GG11 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.2. Configuration Summary

Module	Configuration	Pin Connections
USART0	IrDA, SmartCard	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	I^2S, SmartCard	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	IrDA, SmartCard, High-Speed	US2_TX, US2_RX, US2_CLK, US2_CS
USART3	I^2S, SmartCard	US3_TX, US3_RX, US3_CLK, US3_CS
USART4	I^2S, SmartCard	US4_TX, US4_RX, US4_CLK, US4_CS
USART5	SmartCard	US5_TX, US5_RX, US5_CLK, US5_CS
TIMER0	with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	-	TIM1_CC[3:0]
TIMER2	with DTI	TIM2_CC[2:0], TIM2_CDTI[2:0]
TIMER3	-	TIM3_CC[2:0]
TIMER4	with DTI	TIM4_CC[2:0], TIM4_CDTI[2:0]
TIMER5	-	TIM5_CC[2:0]
TIMER6	with DTI	TIM6_CC[2:0], TIM6_CDTI[2:0]
WTIMER0	with DTI	WTIM0_CC[2:0], WTIM0_CDTI[2:0]
WTIMER1	-	WTIM1_CC[3:0]
WTIMER2	-	WTIM2_CC[2:0]
WTIMER3	-	WTIM3_CC[2:0]

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_{AMB}=25 °C and V_{DD}= 3.3 V, by production test and/or technology characterization.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Refer to 4.1.2.1 General Operating Conditions for more details about operational supply and temperature limits.

4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at http://www.silabs.com/support/quality/pages/default.aspx.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-50	—	150	°C
Voltage on supply pins other than VREGI and VBUS	V_{DDMAX}		-0.3	—	3.8	V
Voltage ramp rate on any supply pin	$V_{DDRAMPMAX}$		—	—	1	V / µs
DC voltage on any GPIO pin	V_{DIGPIN}	5V tolerant GPIO pins[1]	-0.3	—	Min of 5.25 and IOVDD +2	V
		Non-5V tolerant GPIO pins	-0.3	—	IOVDD+0.3	V
Total current into VDD power lines	I_{VDDMAX}	Source	—	—	200	mA
Total current into VSS ground lines	I_{VSSMAX}	Sink	—	—	200	mA
Current per I/O pin	I_{IOMAX}	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	$I_{IOALLMAX}$	Sink	—	—	200	mA
		Source	—	—	200	mA
Junction temperature	T_J	-G grade devices	-40	—	105	°C
Voltage on regulator supply pins VREGI and VBUS	V_{VREGI}		-0.3	—	5.5	V

Note:

1. When a GPIO pin is routed to the analog module through the APORT, the maximum voltage = IOVDD.

4.1.2 Operating Conditions

When assigning supply sources, the following requirements must be observed:

- VREGVDD must be greater than or equal to AVDD, DVDD and all IOVDD supplies.
- VREGVDD = AVDD
- DVDD ≤ AVDD
- IOVDD ≤ AVDD

4.1.2.1 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range	T_A	-G temperature grade	-40	25	85	°C
AVDD supply voltage[3]	V_{AVDD}		1.8	3.3	3.8	V
VREGVDD operating supply voltage[3] [1]	$V_{VREGVDD}$	DCDC in regulation	2.4	3.3	3.8	V
		DCDC in bypass 50mA load	1.8	3.3	3.8	V
		DCDC not in use. DVDD externally shorted to VREGVDD	1.8	3.3	3.8	V
VREGVDD current	$I_{VREGVDD}$	DCDC in bypass	—	—	200	mA
DVDD operating supply voltage	V_{DVDD}		1.62	—	$V_{VREGVDD}$	V
IOVDD operating supply voltage (All IOVDD pins)	V_{IOVDD}		1.62	—	$V_{VREGVDD}$	V
DECOUPLE output capacitor[4]	$C_{DECOUPLE}$		0.75	1.0	2.75	µF
Difference between AVDD and VREGVDD, ABS(AVDD-VREGVDD)[2]	dV_{DD}		—	—	0.1	V
HFCORECLK frequency	f_{CORE}	VSCALE2, MODE = WS3	—	—	72	MHz
		VSCALE2, MODE = WS2	—	—	54	MHz
		VSCALE2, MODE = WS1	—	—	36	MHz
		VSCALE2, MODE = WS0	—	—	18	MHz
		VSCALE0, MODE = WS2	—	—	20	MHz
		VSCALE0, MODE = WS1	—	—	14	MHz
		VSCALE0, MODE = WS0	—	—	7	MHz
HFCLK frequency	f_{HFCLK}	VSCALE2	—	—	72	MHz
		VSCALE0	—	—	20	MHz
HFSRCCLK frequency	$f_{HFSRCCLK}$	VSCALE2	—	—	72	MHz
		VSCALE0	—	—	20	MHz
HFBUSCLK frequency	$f_{HFBUSCLK}$	VSCALE2	—	—	50	MHz
		VSCALE0	—	—	20	MHz
HFPERCLK frequency	$f_{HFPERCLK}$	VSCALE2	—	—	50	MHz
		VSCALE0	—	—	20	MHz
HFPERBCLK frequency	$f_{HFPERBCLK}$	VSCALE2	—	—	72	MHz
		VSCALE0	—	—	20	MHz
HFPERCCLK frequency	$f_{HFPERCCLK}$	VSCALE2	—	—	50	MHz
		VSCALE0	—	—	20	MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. The minimum voltage required in bypass mode is calculated using R_{BYP} from the DCDC specification table. Requirements for other loads can be calculated as $V_{DVDD\_min}+I_{LOAD} * R_{BYP\_max}$.
2. AVDD and VREGVDD pins should be physically shorted.
3. VREGVDD must be tied to AVDD. Both VREGVDD and AVDD minimum voltages must be satisfied for the part to operate. .
4. The system designer should consult the characteristic specs of the capacitor used on DECOUPLE to ensure its capacitance value stays within the specified bounds across temperature and DC bias.

4.1.3 DC-DC Converter

Test conditions: L_DCDC=4.7 µH (Murata LQH3NPN4R7MM0L), C_DCDC=4.7 µF (Samsung CL10B475KQ8NQNC), V_DCDC_I=3.3 V, V_DCDC_O=1.8 V, I_DCDC_LOAD=50 mA, Heavy Drive configuration, F_DCDC_LN=7 MHz, unless otherwise indicated.

Table 4.3. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{DCDC_I}	Bypass mode, I_{DCDC_LOAD} = 50 mA	1.8	—	$V_{VREGVDD\_MAX}$	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 100 mA, or Low power (LP) mode, 1.8 V output, I_{DCDC_LOAD} = 10 mA	2.4	—	$V_{VREGVDD\_MAX}$	V
		Low noise (LN) mode, 1.8 V output, I_{DCDC_LOAD} = 200 mA	2.6	—	$V_{VREGVDD\_MAX}$	V
Output voltage programmable range[1]	V_{DCDC_O}		1.8	—	$V_{VREGVDD}$	V
Regulation DC accuracy	ACC_{DC}	Low Noise (LN) mode, 1.8 V target output	TBD	—	TBD	V
Regulation window[4]	WIN_{REG}	Low Power (LP) mode, LPCMPBIASEMxx[3] = 0, 1.8 V target output, I_{DCDC_LOAD} ≤ 75 µA	TBD	—	TBD	V
		Low Power (LP) mode, LPCMPBIASEMxx[3] = 3, 1.8 V target output, I_{DCDC_LOAD} ≤ 10 mA	TBD	—	TBD	V
Steady-state output ripple	V_R		—	3	—	mVpp
Output voltage under/overshoot	V_{OV}	CCM Mode (LNFORCECCM[3] = 1), Load changes between 0 mA and 100 mA	—	25	TBD	mV
		DCM Mode (LNFORCECCM[3] = 0), Load changes between 0 mA and 10 mA	—	45	TBD	mV
		Overshoot during LP to LN CCM/DCM mode transitions compared to DC level in LN mode	—	200	—	mV
		Undershoot during BYP/LP to LN CCM (LNFORCECCM[3] = 1) mode transitions compared to DC level in LN mode	—	40	—	mV
		Undershoot during BYP/LP to LN DCM (LNFORCECCM[3] = 0) mode transitions compared to DC level in LN mode	—	100	—	mV
DC line regulation	V_{REG}	Input changes between $V_{VREGVDD\_MAX}$ and 2.4 V	—	0.1	—	%
DC load regulation	I_{REG}	Load changes between 0 mA and 100 mA in CCM mode	—	0.1	—	%

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max load current	I_{LOAD_MAX}	Low noise (LN) mode, Heavy Drive[2]	—	—	200	mA
		Low noise (LN) mode, Medium Drive[2]	—	—	100	mA
		Low noise (LN) mode, Light Drive[2]	—	—	50	mA
		Low power (LP) mode, LPCMPBIASEMxx[3] = 0	—	—	75	μA
		Low power (LP) mode, LPCMPBIASEMxx[3] = 3	—	—	10	mA
DCDC nominal output capacitor[5]	C_{DCDC}	25% tolerance	1	4.7	4.7	μF
DCDC nominal output inductor	L_{DCDC}	20% tolerance	4.7	4.7	4.7	μH
Resistance in Bypass mode	R_{BYP}		—	1.2	TBD	Ω

Note:

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, $V_{VREGVDD}$.
2. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.
3. LPCMPBIASEMxx refers to either LPCMPBIASEM234H in the EMU_DCDCMISCCTRL register or LPCMPBIASEM01 in the EMU_DCDCLOEM01CFG register, depending on the energy mode.
4. LP mode controller is a hysteretic controller that maintains the output voltage within the specified limits.
5. Output voltage under/over-shoot and regulation are specified with C_{DCDC} 4.7 μF. Different control loop settings must be used if C_{DCDC} is lower than 4.7 μF.

4.1.4 5V Regulator

Table 4.4. 5V Regulator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VREGI or VBUS input voltage range	V_{VREGI}	Regulating output	2.7	—	5.5	V
		Bypass mode enabled	2.7	—	3.8	V
VREGO output voltage	V_{VREGO}	Regulating output, 3.3 V setting	TBD	3.3	TBD	V
		EM4S open-loop output, I_{OUT} < 100 µA	TBD	—	TBD	V
Voltage output step size	V_{VREGO_SS}		—	0.1	—	V
Bypass mode impedance	R_{BYPASS}	Bypass mode enabled	—	—	TBD	Ω
Output current	I_{OUT}	EM0 or EM1	—	—	200	mA
		EM2, EM3, or EM4H	—	—	2	mA
		EM4S	—	—	20	µA
Load regulation	LR_{VREGO}	EM0 or EM1	—	0.11	—	mV/mA
		EM2, EM3, or EM4H	—	3.5	—	mV/mA
VREGI or VBUS bypass capacitance	C_{VREGI}		TBD	1	TBD	µF
VREGO bypass capacitance	C_{VREGO}		1	4.7	10	µF
Supply current consumption	I_{VREGI}	EM0 or EM1, No load	—	TBD	—	µA
		EM2, EM3, or EM4H, No load	—	TBD	—	nA
		EM4S, No load	—	TBD	—	nA
VREGI and VBUS detection high threshold	V_{DET_H}		TBD	TBD	—	V
VREGI and VBUS detection low threshold	V_{DET_L}		—	TBD	TBD	V
Current monitor transfer ratio	$IMON_{XF}$	Translation of current through VREGO path to voltage at ADC input	—	0.35	—	mA/mV

4.1.5 Backup Supply Domain

Table 4.5. Backup Supply Domain

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Backup supply voltage range	V_{BU_VIN}		TBD	—	3.8	V
PWRRES resistor	R_{PWRRES}	EMU_BUCTRL_PWRRES = RES0	TBD	3900	TBD	Ω
		EMU_BUCTRL_PWRRES = RES1	TBD	1800	TBD	Ω
		EMU_BUCTRL_PWRRES = RES2	TBD	1330	TBD	Ω
		EMU_BUCTRL_PWRRES = RES3	TBD	815	TBD	Ω
Output impedance between BU_VIN and BU_VOUT	R_{BU_VOUT}	EMU_BUCTRL_VOUTRES = STRONG	TBD	110	TBD	Ω
		EMU_BUCTRL_VOUTRES = MED	TBD	775	TBD	Ω
		EMU_BUCTRL_VOUTRES = WEAK	TBD	6500	TBD	Ω
Supply current	I_{BU_VIN}	BU_VIN not powering backup domain	—	TBD	TBD	nA
		BU_VIN powering backup domain[1]	—	TBD	TBD	nA

Note:

1. Additional current required by backup circuitry when backup is active. Includes supply current of backup switches and backup regulator. Does not include supply current required for backed-up circuitry.

4.1.6 Current Consumption

4.1.6.1 Current Consumption 3.3 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 3.3 V. T = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Table 4.6. Current Consumption 3.3 V without DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	72 MHz HFRCO, CPU running Prime from flash	—	120	—	µA/MHz
		72 MHz HFRCO, CPU running while loop from flash	—	120	TBD	µA/MHz
		72 MHz HFRCO, CPU running CoreMark loop from flash	—	140	—	µA/MHz
		50 MHz crystal, CPU running while loop from flash	—	126	—	µA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	122	TBD	µA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	124	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	125	TBD	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	131	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	312	TBD	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled	I_{ACTIVE_VS}	19 MHz HFRCO, CPU running while loop from flash	—	106	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	257	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	72 MHz HFRCO	—	57	TBD	µA/MHz
		50 MHz crystal	—	63	—	µA/MHz
		48 MHz HFRCO	—	59	TBD	µA/MHz
		32 MHz HFRCO	—	61	—	µA/MHz
		26 MHz HFRCO	—	62	TBD	µA/MHz
		16 MHz HFRCO	—	67	—	µA/MHz
		1 MHz HFRCO	—	248	TBD	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled	I_{EM1_VS}	19 MHz HFRCO	—	55	—	µA/MHz
		1 MHz HFRCO	—	206	—	µA/MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM2 mode, with voltage scaling enabled	I_{EM2_VS}	Full 512 kB RAM retention and RTCC running from LFXO	—	3.8	—	μA
		Full 512 kB RAM retention and RTCC running from LFRCO	—	4.0	—	μA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO[2]	—	2.5	TBD	μA
Current consumption in EM3 mode, with voltage scaling enabled	I_{EM3_VS}	Full 512 kB RAM retention and CRYOTIMER running from ULFR-CO	—	3.3	TBD	μA
Current consumption in EM4H mode, with voltage scaling enabled	I_{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	1.0	—	μA
		128 byte RAM retention, CRYO-TIMER running from ULFRCO	—	0.5	—	μA
		128 byte RAM retention, no RTCC	—	0.5	TBD	μA
Current consumption in EM4S mode	I_{EM4S}	No RAM retention, no RTCC	—	0.1	TBD	μA
Current consumption of pe-ripheral power domain 1, with voltage scaling enabled	I_{PD1_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 1 are enabled[1]	—	TBD	—	μA
Current consumption of pe-ripheral power domain 2, with voltage scaling enabled	I_{PD2_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 2 are enabled[1]	—	TBD	—	μA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.2.4 EM2 and EM3 Power Domains for a list of the peripherals in each power domain.
2. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

4.1.6.2 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = 1.8 V DC-DC output. T = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Table 4.7. Current Consumption 3.3 V using DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise DCM mode[2]	I_{ACTIVE_DCM}	72 MHz HFRCO, CPU running Prime from flash	—	77	—	µA/MHz
		72 MHz HFRCO, CPU running while loop from flash	—	78	—	µA/MHz
		72 MHz HFRCO, CPU running CoreMark loop from flash	—	90	—	µA/MHz
		50 MHz crystal, CPU running while loop from flash	—	83	—	µA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	81	—	µA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	87	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	91	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	105	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	655	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise CCM mode[1]	I_{ACTIVE_CCM}	72 MHz HFRCO, CPU running Prime from flash	—	81	—	µA/MHz
		72 MHz HFRCO, CPU running while loop from flash	—	81	—	µA/MHz
		72 MHz HFRCO, CPU running CoreMark loop from flash	—	93	—	µA/MHz
		50 MHz crystal, CPU running while loop from flash	—	90	—	µA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	89	—	µA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	101	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	109	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	137	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1214	—	µA/MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled, DCDC in LP mode[3]	I_{ACTIVE_LPM}	32 MHz HFRCO, CPU running while loop from flash	—	79	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	80	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	84	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	226	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise CCM mode[1]	$I_{ACTIVE\_CCM\_VS}$	19 MHz HFRCO, CPU running while loop from flash	—	113	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1188	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in LP mode[3]	$I_{ACTIVE\_LPM\_VS}$	19 MHz HFRCO, CPU running while loop from flash	—	68	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	190	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Noise DCM mode[2]	I_{EM1_DCM}	72 MHz HFRCO	—	40	—	µA/MHz
		50 MHz crystal	—	45	—	µA/MHz
		48 MHz HFRCO	—	44	—	µA/MHz
		32 MHz HFRCO	—	50	—	µA/MHz
		26 MHz HFRCO	—	54	—	µA/MHz
		16 MHz HFRCO	—	68	—	µA/MHz
		1 MHz HFRCO	—	620	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled, DCDC in Low Power mode[3]	I_{EM1_LPM}	32 MHz HFRCO	—	39	—	µA/MHz
		26 MHz HFRCO	—	40	—	µA/MHz
		16 MHz HFRCO	—	44	—	µA/MHz
		1 MHz HFRCO	—	183	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise DCM mode[2]	$I_{EM1\_DCM\_VS}$	19 MHz HFRCO	—	56	—	µA/MHz
		1 MHz HFRCO	—	595	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled. DCDC in LP mode[3]	$I_{EM1\_LPM\_VS}$	19 MHz HFRCO	—	36	—	µA/MHz
		1 MHz HFRCO	—	158	—	µA/MHz
Current consumption in EM2 mode, with voltage scaling enabled, DCDC in LP mode[3]	I_{EM2_VS}	Full 512 kB RAM retention and RTCC running from LFXO	—	2.5	—	µA
		Full 512 kB RAM retention and RTCC running from LFRCO	—	2.6	—	µA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO[5]	—	1.6	—	µA
Current consumption in EM3 mode, with voltage scaling enabled	I_{EM3_VS}	Full 512 kB RAM retention and CRYOTIMER running from ULFRCO	—	2.2	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM4H mode, with voltage scaling enabled	I_{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	0.8	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.4	—	µA
		128 byte RAM retention, no RTCC	—	0.4	—	µA
Current consumption in EM4S mode	I_{EM4S}	No RAM retention, no RTCC	—	0.1	—	µA
Current consumption of peripheral power domain 1, with voltage scaling enabled, DCDC in LP mode[3]	I_{PD1_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 1 are enabled[4]	—	TBD	—	µA
Current consumption of peripheral power domain 2, with voltage scaling enabled, DCDC in LP mode[3]	I_{PD2_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 2 are enabled[4]	—	TBD	—	µA

Note:

1. DCDC Low Noise CCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=6.4 MHz (RCOBAND=4), ANASW=DVDD.
2. DCDC Low Noise DCM Mode = Light Drive (PFETCNT=NFETCNT=3), F=3.0 MHz (RCOBAND=0), ANASW=DVDD.
3. DCDC Low Power Mode = Medium Drive (PFETCNT=NFETCNT=7), LPOSCDIV=1, LPCMPBIASEM234H=0, LPCLIMILIMSEL=1, ANASW=DVDD.
4. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.2.4 EM2 and EM3 Power Domains for a list of the peripherals in each power domain.
5. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

4.1.6.3 Current Consumption 1.8 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 1.8 V. T = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T = 25 °C.

Table 4.8. Current Consumption 1.8 V without DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	72 MHz HFRCO, CPU running Prime from flash	—	120	—	µA/MHz
		72 MHz HFRCO, CPU running while loop from flash	—	120	—	µA/MHz
		72 MHz HFRCO, CPU running CoreMark loop from flash	—	140	—	µA/MHz
		50 MHz crystal, CPU running while loop from flash	—	125	—	µA/MHz
		48 MHz HFRCO, CPU running while loop from flash	—	121	—	µA/MHz
		32 MHz HFRCO, CPU running while loop from flash	—	124	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	125	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	131	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	309	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled	I_{ACTIVE_VS}	19 MHz HFRCO, CPU running while loop from flash	—	106	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	255	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	72 MHz HFRCO	—	57	—	µA/MHz
		50 MHz crystal	—	62	—	µA/MHz
		48 MHz HFRCO	—	59	—	µA/MHz
		32 MHz HFRCO	—	61	—	µA/MHz
		26 MHz HFRCO	—	62	—	µA/MHz
		16 MHz HFRCO	—	67	—	µA/MHz
		1 MHz HFRCO	—	245	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled	I_{EM1_VS}	19 MHz HFRCO	—	55	—	µA/MHz
		1 MHz HFRCO	—	203	—	µA/MHz
Current consumption in EM2 mode, with voltage scaling enabled	I_{EM2_VS}	Full 512 kB RAM retention and RTCC running from LFXO	—	3.6	—	µA
		Full 512 kB RAM retention and RTCC running from LFRCO	—	3.8	—	µA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO[2]	—	2.3	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM3 mode, with voltage scaling enabled	I_{EM3_VS}	Full 512 kB RAM retention and CRYOTIMER running from ULFR-CO	—	3.2	—	μA
Current consumption in EM4H mode, with voltage scaling enabled	I_{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	0.9	—	μA
		128 byte RAM retention, CRYO-TIMER running from ULFRCO	—	0.4	—	μA
		128 byte RAM retention, no RTCC	—	0.4	—	μA
Current consumption in EM4S mode	I_{EM4S}	No RAM retention, no RTCC	—	0.1	—	μA
Current consumption of pe-ripheral power domain 1, with voltage scaling enabled	I_{PD1_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 1 are enabled[1]	—	TBD	—	μA
Current consumption of pe-ripheral power domain 2, with voltage scaling enabled	I_{PD2_VS}	Additional current consumption in EM2/3 when any peripherals on power domain 2 are enabled[1]	—	TBD	—	μA

Note:

1. Extra current consumed by power domain. Does not include current associated with the enabled peripherals. See 3.2.4 EM2 and EM3 Power Domains for a list of the peripherals in each power domain.
2. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1

4.1.7 Wake Up Times

Table 4.9. Wake Up Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wakeup time from EM1	t_{EM1_WU}		—	3	—	AHB Clocks
Wake up from EM2	t_{EM2_WU}	Code execution from flash	—	10.9	—	µs
		Code execution from RAM	—	3.8	—	µs
Wake up from EM3	t_{EM3_WU}	Code execution from flash	—	10.9	—	µs
		Code execution from RAM	—	3.8	—	µs
Wake up from EM4H[1]	t_{EM4H_WU}	Executing from flash	—	90	—	µs
Wake up from EM4S[1]	t_{EM4S_WU}	Executing from flash	—	300	—	µs
Time from release of reset source to first instruction execution	t_{RESET}	Soft Pin Reset released	—	51	—	µs
		Any other reset released	—	358	—	µs
Power mode scaling time	t_{SCALE}	VSCALE0 to VSCALE2, HFCLK = 19 MHz[4] [2]	—	31.8	—	µs
		VSCALE2 to VSCALE0, HFCLK = 19 MHz[3]	—	4.3	—	µs

Note:

1. Time from wakeup request until first instruction is executed. Wakeup results in device reset.
2. VSCALE0 to VSCALE2 voltage change transitions occur at a rate of 10 mV/µs for approximately 20 µs. During this transition, peak currents will be dependent on the value of the DECOUPLE output capacitor, from 35 mA (with a 1 µF capacitor) to 70 mA (with a 2.7 µF capacitor).
3. Scaling down from VSCALE2 to VSCALE0 requires approximately 2.8 µs + 29 HFCLKs.
4. Scaling up from VSCALE0 to VSCALE2 requires approximately 30.3 µs + 28 HFCLKs.

4.1.8 Brown Out Detector (BOD)

Table 4.10. Brown Out Detector (BOD)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DVDD BOD threshold	$V_{DVDDBOD}$	DVDD rising	—	—	TBD	V
		DVDD falling (EM0/EM1)	TBD	—	—	V
		DVDD falling (EM2/EM3)	TBD	—	—	V
DVDD BOD hysteresis	$V_{DVDDBOD\_HYST}$		—	18	—	mV
DVDD BOD response time	$t_{DVDDBOD\_DELAY}$	Supply drops at 0.1V/μs rate	—	2.4	—	μs
AVDD BOD threshold	$V_{AVDDBOD}$	AVDD rising	—	—	TBD	V
		AVDD falling (EM0/EM1)	TBD	—	—	V
		AVDD falling (EM2/EM3)	TBD	—	—	V
AVDD BOD hysteresis	$V_{AVDDBOD\_HYST}$		—	20	—	mV
AVDD BOD response time	$t_{AVDDBOD\_DELAY}$	Supply drops at 0.1V/μs rate	—	2.4	—	μs
EM4 BOD threshold	$V_{EM4DBOD}$	AVDD rising	—	—	TBD	V
		AVDD falling	TBD	—	—	V
EM4 BOD hysteresis	V_{EM4BOD_HYST}		—	25	—	mV
EM4 BOD response time	t_{EM4BOD_DELAY}	Supply drops at 0.1V/μs rate	—	300	—	μs

4.1.9 Oscillators

4.1.9.1 Low-Frequency Crystal Oscillator (LFXO)

Table 4.11. Low-Frequency Crystal Oscillator (LFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{LFXO}		—	32.768	—	kHz
Supported crystal equivalent series resistance (ESR)	ESR_{LFXO}		—	—	70	kΩ
Supported range of crystal load capacitance [1]	C_{LFXO_CL}		6	—	18	pF
On-chip tuning cap range [2]	C_{LFXO_T}	On each of LFXTAL_N and LFXTAL_P pins	8	—	40	pF
On-chip tuning cap step size	SS_{LFXO}		—	0.25	—	pF
Current consumption after startup [3]	I_{LFXO}	ESR = 70 kOhm, C_L = 7 pF, GAIN[4] = 2, AGC[4] = 1	—	273	—	nA
Start- up time	t_{LFXO}	ESR = 70 kOhm, C_L = 7 pF, GAIN[4] = 2	—	308	—	ms

Note:

1. Total load capacitance as seen by the crystal.
2. The effective load capacitance seen by the crystal will be C_{LFXO_T} /2. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.
3. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.
4. In CMU_LFXOCTRL register.

4.1.9.2 High-Frequency Crystal Oscillator (HFXO)

Table 4.12. High-Frequency Crystal Oscillator (HFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{HFXO}		4	—	50	MHz
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO}	50 MHz crystal	—	—	TBD	Ω
		TBD MHz crystal	—	—	TBD	Ω
		4 MHz crystal	—	—	TBD	Ω
Supported range of crystal load capacitance[1]	C_{HFXO_CL}		TBD	—	TBD	pF
On-chip tuning cap range[2]	C_{HFXO_T}	On each of HFXTAL_N and HFXTAL_P pins	TBD	—	TBD	pF
On-chip tuning capacitance step	SS_{HFXO}		—	TBD	—	pF
Startup time	t_{HFXO}	50 MHz crystal, ESR = TBD Ohm, C_L = TBD pF	—	TBD	—	µs
		TBD MHz crystal, ESR = TBD Ohm, C_L = TBD pF	—	TBD	—	µs
		4 MHz crystal, ESR = TBD Ohm, C_L = TBD pF	—	TBD	—	µs
Current consumption after startup	I_{HFXO}	50 MHz crystal	—	TBD	—	µA
		TBD MHz crystal	—	TBD	—	µA
		4 MHz crystal	—	TBD	—	µA

Note:

1. Total load capacitance as seen by the crystal.
2. The effective load capacitance seen by the crystal will be C_{HFXO_T} /2. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal.

4.1.9.3 Low-Frequency RC Oscillator (LFRCO)

Table 4.13. Low-Frequency RC Oscillator (LFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{LFRCO}	ENVREF[2] = 1	TBD	32.768	TBD	kHz
		ENVREF[2] = 0	TBD	32.768	TBD	kHz
Startup time	t_{LFRCO}		—	500	—	µs
Current consumption [1]	I_{LFRCO}	ENVREF = 1 in CMU_LFRCOCTRL	—	370	—	nA
		ENVREF = 0 in CMU_LFRCOCTRL	—	520	—	nA

Note:

1. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.
2. In CMU_LFRCOCTRL register.

4.1.9.4 High-Frequency RC Oscillator (HFRCO)

Table 4.14. High-Frequency RC Oscillator (HFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency accuracy	f_{HFRCO_ACC}	At production calibrated frequencies, across supply voltage and temperature	TBD	—	TBD	%
Start-up time	t_{HFRCO}	$f_{HFRCO} \geq 19$ MHz	—	300	—	ns
		$4 < f_{HFRCO} < 19$ MHz	—	1	—	µs
		$f_{HFRCO} \leq 4$ MHz	—	2.5	—	µs
Current consumption on all supplies	I_{HFRCO}	f_{HFRCO} = 72 MHz	—	608	TBD	µA
		f_{HFRCO} = 64 MHz	—	545	TBD	µA
		f_{HFRCO} = 56 MHz	—	478	TBD	µA
		f_{HFRCO} = 48 MHz	—	413	TBD	µA
		f_{HFRCO} = 38 MHz	—	341	TBD	µA
		f_{HFRCO} = 32 MHz	—	286	TBD	µA
		f_{HFRCO} = 26 MHz	—	240	TBD	µA
		f_{HFRCO} = 19 MHz	—	191	TBD	µA
		f_{HFRCO} = 16 MHz	—	164	TBD	µA
		f_{HFRCO} = 13 MHz	—	143	TBD	µA
		f_{HFRCO} = 7 MHz	—	103	TBD	µA
		f_{HFRCO} = 4 MHz	—	42	TBD	µA
		f_{HFRCO} = 2 MHz	—	33	TBD	µA
		f_{HFRCO} = 1 MHz	—	28	TBD	µA
		f_{HFRCO} = 72 MHz, DPLL enabled	—	TBD	TBD	µA
		f_{HFRCO} = 40 MHz, DPLL enabled	—	526	TBD	µA
		f_{HFRCO} = 32 MHz, DPLL enabled	—	419	TBD	µA
		f_{HFRCO} = 16 MHz, DPLL enabled	—	233	TBD	µA
		f_{HFRCO} = 4 MHz, DPLL enabled	—	59	TBD	µA
		f_{HFRCO} = 1 MHz, DPLL enabled	—	36	TBD	µA
Coarse trim step size (% of period)	SS_{HFRCO_COARSE}		—	0.8	—	%
Fine trim step size (% of period)	SS_{HFRCO_FINE}		—	0.1	—	%
Period jitter	PJ_{HFRCO}		—	0.2	—	% RMS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency limits	f_{HFRCO_BAND}	FREQRANGE = 0	TBD	—	TBD	MHz
		FREQRANGE = 1	TBD	—	TBD	MHz
		FREQRANGE = 2	TBD	—	TBD	MHz
		FREQRANGE = 3	TBD	—	TBD	MHz
		FREQRANGE = 4	TBD	—	TBD	MHz
		FREQRANGE = 5	TBD	—	TBD	MHz
		FREQRANGE = 6	TBD	—	TBD	MHz
		FREQRANGE = 7	TBD	—	TBD	MHz
		FREQRANGE = 8	TBD	—	TBD	MHz
		FREQRANGE = 9	TBD	—	TBD	MHz
		FREQRANGE = 10	TBD	—	TBD	MHz
		FREQRANGE = 11	TBD	—	TBD	MHz

4.1.9.5 Auxiliary High-Frequency RC Oscillator (AUXHFRCO)

Table 4.15. Auxiliary High-Frequency RC Oscillator (AUXHFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency accuracy	$f_{AUXHFRCO\_ACC}$	At production calibrated frequencies, across supply voltage and temperature	TBD	—	TBD	%
Start-up time	$t_{AUXHFRCO}$	$f_{AUXHFRCO}$ ≥ 19 MHz	—	400	—	ns
		4 < $f_{AUXHFRCO}$ < 19 MHz	—	1.4	—	µs
		$f_{AUXHFRCO}$ ≤ 4 MHz	—	2.5	—	µs
Current consumption on all supplies	$I_{AUXHFRCO}$	$f_{AUXHFRCO}$ = 50 MHz	—	289	TBD	µA
		$f_{AUXHFRCO}$ = 48 MHz	—	276	TBD	µA
		$f_{AUXHFRCO}$ = 38 MHz	—	227	TBD	µA
		$f_{AUXHFRCO}$ = 32 MHz	—	186	TBD	µA
		$f_{AUXHFRCO}$ = 26 MHz	—	158	TBD	µA
		$f_{AUXHFRCO}$ = 19 MHz	—	126	TBD	µA
		$f_{AUXHFRCO}$ = 16 MHz	—	114	TBD	µA
		$f_{AUXHFRCO}$ = 13 MHz	—	88	TBD	µA
		$f_{AUXHFRCO}$ = 7 MHz	—	59	TBD	µA
		$f_{AUXHFRCO}$ = 4 MHz	—	33	TBD	µA
		$f_{AUXHFRCO}$ = 2 MHz	—	28	TBD	µA
		$f_{AUXHFRCO}$ = 1 MHz	—	26	TBD	µA
Coarse trim step size (% of period)	$SS_{AUXHFRCO\_COARSE}$		—	0.8	—	%
Fine trim step size (% of period)	$SS_{AUXHFRCO\_FINE}$		—	0.1	—	%
Period jitter	$PJ_{AUXHFRCO}$		—	0.2	—	% RMS

4.1.9.6 USB High-Frequency RC Oscillator (USHFRCO)

Table 4.16. USB High-Frequency RC Oscillator (USHFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency accuracy	$f_{USHFRCO\_ACC}$	At production calibrated frequencies, across supply voltage and temperature	TBD	—	TBD	%
		USB clock recovery enabled, Active connection as device	-0.25	—	0.25	%
Start-up time	$t_{USHFRCO}$		—	TBD	—	ns
Current consumption on all supplies	$I_{USHFRCO}$	$f_{USHFRCO}$ = 50 MHz	—	342	TBD	µA
		$f_{USHFRCO}$ = 48 MHz	—	318	TBD	µA
		$f_{USHFRCO}$ = 32 MHz	—	223	TBD	µA
		$f_{USHFRCO}$ = 16 MHz	—	132	TBD	µA
Duty cycle	$DC_{USHFRCO}$		—	TBD	—	%
Period jitter	$PJ_{USHFRCO}$		TBD	—	TBD	% RMS

4.1.9.7 Ultra-low Frequency RC Oscillator (ULFRCO)

Table 4.17. Ultra-low Frequency RC Oscillator (ULFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{ULFRCO}		TBD	1	TBD	kHz

4.1.10 Flash Memory Characteristics[5]

Table 4.18. Flash Memory Characteristics[5]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC_{FLASH}		10000	—	—	cycles
Flash data retention	RET_{FLASH}		10	—	—	years
Word (32-bit) programming time	t_{W_PROG}	Burst write, 128 words, average time per word	20	TBD	30	µs
		Single word	60	TBD	80	µs
Page erase time[4]	t_{PERASE}		20	TBD	35	ms
Mass erase time[1]	t_{MERASE}		20	TBD	35	ms
Device erase time[2 3]	t_{DERASE}		—	TBD	TBD	ms
Erase current[6]	I_{ERASE}	Page Erase	—	—	TBD	mA
		Mass or Device Erase	—	—	TBD	mA
Write current[6]	I_{WRITE}		—	—	TBD	mA
Supply voltage during flash erase and write	V_{FLASH}		1.62	—	3.6	V

Note:

1. Mass erase is issued by the CPU and erases all flash.
2. Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW).
3. From setting the DEVICEERASE bit in AAP_CMD to 1 until the ERASEBUSY bit in AAP_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
4. From setting the ERASEPAGE bit in MSC_WRITECMD to 1 until the BUSY bit in MSC_STATUS is cleared to 0. Internal setup and hold times for flash control signals are included.
5. Flash data retention information is published in the Quarterly Quality and Reliability Report.
6. Measured at 25 °C.

4.1.11 General-Purpose I/O (GPIO)

Table 4.19. General-Purpose I/O (GPIO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IL}	GPIO pins	—	—	IOVDD*0.3	V
Input high voltage	V_{IH}	GPIO pins	IOVDD*0.7	—	—	V
Output high voltage relative to IOVDD	V_{OH}	Sourcing 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK	IOVDD*0.8	—	—	V
		Sourcing 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK	IOVDD*0.6	—	—	V
		Sourcing 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG	IOVDD*0.8	—	—	V
		Sourcing 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG	IOVDD*0.6	—	—	V
Output low voltage relative to IOVDD	V_{OL}	Sinking 3 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = WEAK	—	—	IOVDD*0.2	V
		Sinking 1.2 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = WEAK	—	—	IOVDD*0.4	V
		Sinking 20 mA, IOVDD ≥ 3 V, DRIVESTRENGTH[1] = STRONG	—	—	IOVDD*0.2	V
		Sinking 8 mA, IOVDD ≥ 1.62 V, DRIVESTRENGTH[1] = STRONG	—	—	IOVDD*0.4	V
Input leakage current	I_{IOLEAK}	All GPIO except LFXO pins, GPIO ≤ IOVDD	—	0.1	TBD	nA
		LFXO Pins, GPIO ≤ IOVDD	—	0.1	TBD	nA
Input leakage current on 5VTOL pads above IOVDD	$I_{5VTOLLEAK}$	IOVDD < GPIO ≤ IOVDD + 2 V	—	3.3	TBD	µA
I/O pin pull-up/pull-down resistor	R_{PUD}		TBD	40	TBD	kΩ
Pulse width of pulses removed by the glitch suppression filter	$t_{IOGLITCH}$		TBD	25	TBD	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output fall time, From 70% to 30% of V_{IO}	t_{IOOF}	C_L = 50 pF, DRIVESTRENGTH[1] = STRONG, SLEWRATE[1] = 0x6	—	1.8	—	ns
		C_L = 50 pF, DRIVESTRENGTH[1] = WEAK, SLEWRATE[1] = 0x6	—	4.5	—	ns
Output rise time, From 30% to 70% of V_{IO}	t_{IOOR}	C_L = 50 pF, DRIVESTRENGTH[1] = STRONG, SLEWRATE = 0x6[1]	—	2.2	—	ns
		C_L = 50 pF, DRIVESTRENGTH[1] = WEAK, SLEWRATE[1] = 0x6	—	7.4	—	ns

Note:

1. In GPIO_Pn_CTRL register.

4.1.12 Voltage Monitor (VMON)

Table 4.20. Voltage Monitor (VMON)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current (including I_SENSE)	I_{VMON}	In EM0 or EM1, 1 supply monitored	—	6.0	TBD	μA
		In EM0 or EM1, 4 supplies monitored	—	14.9	TBD	μA
		In EM2, EM3 or EM4, 1 supply monitored and above threshold	—	62	—	nA
		In EM2, EM3 or EM4, 1 supply monitored and below threshold	—	62	—	nA
		In EM2, EM3 or EM4, 4 supplies monitored and all above threshold	—	99	—	nA
		In EM2, EM3 or EM4, 4 supplies monitored and all below threshold	—	99	—	nA
Loading of monitored supply	I_{SENSE}	In EM0 or EM1	—	2	—	μA
		In EM2, EM3 or EM4	—	2	—	nA
Threshold range	V_{VMON_RANGE}		1.62	—	3.4	V
Threshold step size	N_{VMON_STESP}	Coarse	—	200	—	mV
		Fine	—	20	—	mV
Response time	t_{VMON_RES}	Supply drops at 1V/μs rate	—	460	—	ns
Hysteresis	V_{VMON_HYST}		—	26	—	mV

4.1.13 Analog to Digital Converter (ADC)

Specified at 1 Msps, ADCCLK = 16 MHz, BIASPROG = 0, GPBIASACC = 0, unless otherwise indicated.

Table 4.21. Analog to Digital Converter (ADC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	$V_{RESOLUTION}$		6	—	12	Bits
Input voltage range[5]	V_{ADCIN}	Single ended	—	—	V_{FS}	V
		Differential	$-V_{FS}/2$	—	$V_{FS}/2$	V
Input range of external reference voltage, single ended and differential	$V_{ADCREFIN\_P}$		1	—	V_{AVDD}	V
Power supply rejection[2]	$PSRR_{ADC}$	At DC	—	80	—	dB
Analog input common mode rejection ratio	$CMRR_{ADC}$	At DC	—	80	—	dB
Current from all supplies, using internal reference buffer. Continous operation. WARMUPMODE[4] = KEEPADCWARM	$I_{ADC\_CONTINOUS\_LP}$	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	270	TBD	μA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 1 [3]	—	125	—	μA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 1 [3]	—	80	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE[4] = NORMAL	$I_{ADC\_NORMAL\_LP}$	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	45	—	μA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 1 [3]	—	8	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[4] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADC\_STANDBY\_LP}$	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	105	—	μA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 1 [3]	—	70	—	μA
Current from all supplies, using internal reference buffer. Continous operation. WARMUPMODE[4] = KEEPADCWARM	$I_{ADC\_CONTINOUS\_HP}$	1 Msps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	325	—	μA
		250 ksps / 4 MHz ADCCLK, BIASPROG = 6, GPBIASACC = 0 [3]	—	175	—	μA
		62.5 ksps / 1 MHz ADCCLK, BIASPROG = 15, GPBIASACC = 0 [3]	—	125	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. WARMUPMODE[4] = NORMAL	$I_{ADC\_NORMAL\_HP}$	35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	85	—	μA
		5 ksps / 16 MHz ADCCLK BIASPROG = 0, GPBIASACC = 0 [3]	—	16	—	μA
Current from all supplies, using internal reference buffer. Duty-cycled operation. AWARMUPMODE[4] = KEEPINSTANDBY or KEEPINSLOWACC	$I_{ADC\_STANDBY\_HP}$	125 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	160	—	μA
		35 ksps / 16 MHz ADCCLK, BIASPROG = 0, GPBIASACC = 0 [3]	—	125	—	μA
Current from HFPERCLK	I_{ADC_CLK}	HFPERCLK = 16 MHz	—	180	—	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC clock frequency	f_{ADCCLK}		—	—	16	MHz
Throughput rate	$f_{ADCRATE}$		—	—	1	Msps
Conversion time[1]	$t_{ADCCONV}$	6 bit	—	7	—	cycles
		8 bit	—	9	—	cycles
		12 bit	—	13	—	cycles
Startup time of reference generator and ADC core	$t_{ADCSTART}$	WARMUPMODE[4] = NORMAL	—	—	5	μs
		WARMUPMODE[4] = KEEPIN-STANDBY	—	—	2	μs
		WARMUPMODE[4] = KEEPINSLO-WACC	—	—	1	μs
SNDR at 1Msps and f_{IN} = 10kHz	$SNDR_{ADC}$	Internal reference[7], differential measurement	TBD	67	—	dB
		External reference[6], differential measurement	—	68	—	dB
Spurious-free dynamic range (SFDR)	$SFDR_{ADC}$	1 MSamples/s, 10 kHz full-scale sine wave	—	75	—	dB
Differential non-linearity (DNL)	DNL_{ADC}	12 bit resolution, No missing co-des	TBD	—	TBD	LSB
Integral non-linearity (INL), End point method	INL_{ADC}	12 bit resolution	TBD	—	TBD	LSB
Offset error	$V_{ADCOFFSETERR}$		TBD	0	TBD	LSB
Gain error in ADC	$V_{ADCGAIN}$	Using internal reference	—	-0.2	TBD	%
		Using external reference	—	-1	—	%
Temperature sensor slope	V_{TS_SLOPE}		—	-1.84	—	mV/°C

Note:

1. Derived from ADCCLK.
2. PSRR is referenced to AVDD when ANASW=0 and to DVDD when ANASW=1 in EMU_PWRCTRL.
3. In ADCn_BIASPROG register.
4. In ADCn_CNTL register.
5. The absolute voltage allowed at any ADC input is dictated by the power rail supplied to on-chip circuitry, and may be lower than the effective full scale voltage. All ADC inputs are limited to the ADC supply (AVDD or DVDD depending on EMU_PWRCTRL_ANASW). Any ADC input routed through the APORT will further be limited by the IOVDD supply to the pin.
6. External reference is 1.25 V applied externally to ADCnEXTREFP, with the selection CONF in the SINGLECTRL_REF or SCANCTRL_REF register field and VREFP in the SINGLECTRLX_VREFSEL or SCANCTRLX_VREFSEL field. The differential input range with this configuration is ± 1.25 V.
7. Internal reference option used corresponds to selection 2V5 in the SINGLECTRL_REF or SCANCTRL_REF register field. The differential input range with this configuration is ± 1.25 V. Typical value is characterized using full-scale sine wave input. Minimum value is production-tested using sine wave input at 1.5 dB lower than full scale.

4.1.14 Analog Comparator (ACMP)

Table 4.22. Analog Comparator (ACMP)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{ACMPIN}	ACMPVDD = ACMPn_CTRL_PWRSEL [1]	—	—	$V_{ACMPVDD}$	V
Supply voltage	$V_{ACMPVDD}$	BIASPROG[4] ≤ 0x10 or FULL-BIAS[4] = 0	1.8	—	$V_{VREGVDD\_MAX}$	V
		0x10 < BIASPROG[4] ≤ 0x20 and FULLBIAS[4] = 1	2.1	—	$V_{VREGVDD\_MAX}$	V
Active current not including voltage reference[2]	I_{ACMP}	BIASPROG[4] = 1, FULLBIAS[4] = 0	—	50	—	nA
		BIASPROG[4] = 0x10, FULLBIAS[4] = 0	—	306	—	nA
		BIASPROG[4] = 0x02, FULLBIAS[4] = 1	—	6.5	—	µA
		BIASPROG[4] = 0x20, FULLBIAS[4] = 1	—	74	TBD	µA
Current consumption of internal voltage reference[2]	$I_{ACMPREF}$	VLP selected as input using 2.5 V Reference / 4 (0.625 V)	—	50	—	nA
		VLP selected as input using VDD	—	20	—	nA
		VBDIV selected as input using 1.25 V reference / 1	—	4.1	—	µA
		VADIV selected as input using VDD/1	—	2.4	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Hysteresis (V_{CM} = 1.25 V, BIASPROG[4] = 0x10, FULL-BIAS[4] = 1)	$V_{ACMPHYST}$	HYSTSEL[5] = HYST0	TBD	0	TBD	mV
		HYSTSEL[5] = HYST1	TBD	18	TBD	mV
		HYSTSEL[5] = HYST2	TBD	33	TBD	mV
		HYSTSEL[5] = HYST3	TBD	46	TBD	mV
		HYSTSEL[5] = HYST4	TBD	57	TBD	mV
		HYSTSEL[5] = HYST5	TBD	68	TBD	mV
		HYSTSEL[5] = HYST6	TBD	79	TBD	mV
		HYSTSEL[5] = HYST7	TBD	90	TBD	mV
		HYSTSEL[5] = HYST8	TBD	0	TBD	mV
		HYSTSEL[5] = HYST9	TBD	-18	TBD	mV
		HYSTSEL[5] = HYST10	TBD	-33	TBD	mV
		HYSTSEL[5] = HYST11	TBD	-45	TBD	mV
		HYSTSEL[5] = HYST12	TBD	-57	TBD	mV
		HYSTSEL[5] = HYST13	TBD	-67	TBD	mV
		HYSTSEL[5] = HYST14	TBD	-78	TBD	mV
		HYSTSEL[5] = HYST15	TBD	-88	TBD	mV
Comparator delay[3]	$t_{ACMPDELAY}$	BIASPROG[4] = 1, FULLBIAS[4] = 0	—	30	—	μs
		BIASPROG[4] = 0x10, FULLBIAS[4] = 0	—	3.7	—	μs
		BIASPROG[4] = 0x02, FULLBIAS[4] = 1	—	360	—	ns
		BIASPROG[4] = 0x20, FULLBIAS[4] = 1	—	35	—	ns
Offset voltage	$V_{ACMPOFFSET}$	BIASPROG[4] =0x10, FULLBIAS[4] = 1	TBD	—	TBD	mV
Reference voltage	$V_{ACMPREF}$	Internal 1.25 V reference	TBD	1.25	TBD	V
		Internal 2.5 V reference	TBD	2.5	TBD	V
Capacitive sense internal resistance	R_{CSRES}	CSRESSEL[6] = 0	—	infinite	—	kΩ
		CSRESSEL[6] = 1	—	15	—	kΩ
		CSRESSEL[6] = 2	—	27	—	kΩ
		CSRESSEL[6] = 3	—	39	—	kΩ
		CSRESSEL[6] = 4	—	51	—	kΩ
		CSRESSEL[6] = 5	—	100	—	kΩ
		CSRESSEL[6] = 6	—	162	—	kΩ
		CSRESSEL[6] = 7	—	235	—	kΩ

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:
1. ACMPVDD is a supply chosen by the setting in ACMPn_CTRL_PWRSEL and may be IOVDD, AVDD or DVDD.
2. The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference. $I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$.
3. ± 100 mV differential drive.
4. In ACMPn_CTRL register.
5. In ACMPn_HYSTERESIS register.
6. In ACMPn_INPUTSEL register.

4.1.15 Digital to Analog Converter (VDAC)

DRIVESTRENGTH = 2 unless otherwise specified. Primary VDAC output.

Table 4.23. Digital to Analog Converter (VDAC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output voltage	V_{DACOUT}	Single-Ended	0	—	V_{VREF}	V
		Differential[2]	$-V_{VREF}$	—	V_{VREF}	V
Current consumption including references (2 channels)[1]	I_{DAC}	500 ksps, 12-bit, DRIVESTRENGTH = 2, REFSEL = 4	—	396	—	μA
		44.1 ksps, 12-bit, DRIVESTRENGTH = 1, REFSEL = 4	—	88	—	μA
		200 Hz refresh rate, 12-bit Sample-Off mode in EM2, DRIVESTRENGTH = 2, BGRREQTIME = 1, EM2REFENTIME = 9, REFSEL = 4, SETTLETIME = 0x0A, WARMUPTIME = 0x02	—	2	—	μA
Current from HFPERCLK[4]	I_{DAC_CLK}		—	5.8	—	μA/MHz
Sample rate	SR_{DAC}		—	—	500	ksps
DAC clock frequency	f_{DAC}		—	—	1	MHz
Conversion time	$t_{DACCONV}$	f_{DAC} = 1MHz	2	—	—	μs
Settling time	$t_{DACSETTLE}$	50% fs step settling to 5 LSB	—	2.5	—	μs
Startup time	$t_{DACSTARTUP}$	Enable to 90% fs output, settling to 10 LSB	—	—	12	μs
Output impedance	R_{OUT}	DRIVESTRENGTH = 2, 0.4 V ≤ V_{OUT} ≤ V_{OPA} - 0.4 V, -8 mA < I_{OUT} < 8 mA, Full supply range	—	2	—	Ω
		DRIVESTRENGTH = 0 or 1, 0.4 V ≤ V_{OUT} ≤ V_{OPA} - 0.4 V, -400 μA < I_{OUT} < 400 μA, Full supply range	—	2	—	Ω
		DRIVESTRENGTH = 2, 0.1 V ≤ V_{OUT} ≤ V_{OPA} - 0.1 V, -2 mA < I_{OUT} < 2 mA, Full supply range	—	2	—	Ω
		DRIVESTRENGTH = 0 or 1, 0.1 V ≤ V_{OUT} ≤ V_{OPA} - 0.1 V, -100 μA < I_{OUT} < 100 μA, Full supply range	—	2	—	Ω
Power supply rejection ratio[6]	PSRR	Vout = 50% fs. DC	—	65.5	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 250 kHz	$SNDR_{DAC}$	500 ksps, single-ended, internal 1.25V reference	—	60.4	—	dB
		500 ksps, single-ended, internal 2.5V reference	—	61.6	—	dB
		500 ksps, single-ended, 3.3V VDD reference	—	64.0	—	dB
		500 ksps, differential, internal 1.25V reference	—	63.3	—	dB
		500 ksps, differential, internal 2.5V reference	—	64.4	—	dB
		500 ksps, differential, 3.3V VDD reference	—	65.8	—	dB
Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 22 kHz	$SNDR_{DAC\_BAND}$	500 ksps, single-ended, internal 1.25V reference	—	65.3	—	dB
		500 ksps, single-ended, internal 2.5V reference	—	66.7	—	dB
		500 ksps, differential, 3.3V VDD reference	—	68.5	—	dB
		500 ksps, differential, internal 1.25V reference	—	67.8	—	dB
		500 ksps, differential, internal 2.5V reference	—	69.0	—	dB
		500 ksps, single-ended, 3.3V VDD reference	—	70.0	—	dB
Total harmonic distortion	THD		—	70.2	—	dB
Differential non-linearity[3]	DNL_{DAC}		TBD	—	TBD	LSB
Intergral non-linearity	INL_{DAC}		TBD	—	TBD	LSB
Offset error[5]	V_{OFFSET}	T = 25 °C	TBD	—	TBD	mV
		Across operating temperature range	TBD	—	TBD	mV
Gain error[5]	V_{GAIN}	T = 25 °C, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN)	TBD	—	TBD	%
		Across operating temperature range, Low-noise internal reference (REFSEL = 1V25LN or 2V5LN)	TBD	—	TBD	%
External load capactiance, OUTSCALE=0	C_{LOAD}		—	—	75	pF

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Supply current specifications are for VDAC circuitry operating with static output only and do not include current required to drive the load.
2. In differential mode, the output is defined as the difference between two single-ended outputs. Absolute voltage on each output is limited to the single-ended range.
3. Entire range is monotonic and has no missing codes.
4. Current from HFPERCLK is dependent on HFPERCLK frequency. This current contributes to the total supply current used when the clock to the DAC module is enabled in the CMU.
5. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain.
6. PSRR calculated as 20 * $\log_{10}(\Delta VDD / \Delta V_{OUT})$, VDAC output at 90% of full scale

4.1.16 Current Digital to Analog Converter (IDAC)

Table 4.24. Current Digital to Analog Converter (IDAC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Number of ranges	N_{IDAC_RANGES}		—	4	—	ranges
Output current	I_{IDAC_OUT}	RANGSEL[1] = RANGE0	0.05	—	1.6	µA
		RANGSEL[1] = RANGE1	1.6	—	4.7	µA
		RANGSEL[1] = RANGE2	0.5	—	16	µA
		RANGSEL[1] = RANGE3	2	—	64	µA
Linear steps within each range	N_{IDAC_STEPS}		—	32	—	steps
Step size	SS_{IDAC}	RANGSEL[1] = RANGE0	—	50	—	nA
		RANGSEL[1] = RANGE1	—	100	—	nA
		RANGSEL[1] = RANGE2	—	500	—	nA
		RANGSEL[1] = RANGE3	—	2	—	µA
Total accuracy, STEPSEL[1] = 0x80	ACC_{IDAC}	EM0 or EM1, AVDD=3.3 V, T = 25 °C	TBD	—	TBD	%
		EM0 or EM1, Across operating temperature range	TBD	—	TBD	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE0, AVDD=3.3 V, T = 25 °C	—	-2	—	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE1, AVDD=3.3 V, T = 25 °C	—	-1.7	—	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE2, AVDD=3.3 V, T = 25 °C	—	-0.8	—	%
		EM2 or EM3, Source mode, RANGSEL[1] = RANGE3, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
		EM2 or EM3, Sink mode, RANGSEL[1] = RANGE0, AVDD=3.3 V, T = 25 °C	—	-0.7	—	%
		EM2 or EM3, Sink mode, RANGSEL[1] = RANGE1, AVDD=3.3 V, T = 25 °C	—	-0.6	—	%
		EM2 or EM3, Sink mode, RANGSEL[1] = RANGE2, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%
		EM2 or EM3, Sink mode, RANGSEL[1] = RANGE3, AVDD=3.3 V, T = 25 °C	—	-0.5	—	%

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Start up time	t_{IDAC_SU}	Output within 1% of steady state value	—	5	—	μs
Settling time, (output settled within 1% of steady state value),	t_{IDAC_SETTLE}	Range setting is changed	—	5	—	μs
		Step value is changed	—	1	—	μs
Current consumption[2]	I_{IDAC}	EM0 or EM1 Source mode, excluding output current, Across operating temperature range	—	11	TBD	μA
		EM0 or EM1 Sink mode, excluding output current, Across operating temperature range	—	13	TBD	μA
		EM2 or EM3 Source mode, excluding output current, T = 25 °C	—	0.023	—	μA
		EM2 or EM3 Sink mode, excluding output current, T = 25 °C	—	0.041	—	μA
		EM2 or EM3 Source mode, excluding output current, T ≥ 85 °C	—	11	—	μA
		EM2 or EM3 Sink mode, excluding output current, T ≥ 85 °C	—	13	—	μA
Output voltage compliance in source mode, source current change relative to current sourced at 0 V	I_{COMP_SRC}	RANGESEL1=0, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-100 mv)	—	0.11	—	%
		RANGESEL1=1, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-100 mV)	—	0.06	—	%
		RANGESEL1=2, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-150 mV)	—	0.04	—	%
		RANGESEL1=3, output voltage = min(V_{IOVDD}, V_{AVDD}[2]-250 mV)	—	0.03	—	%
Output voltage compliance in sink mode, sink current change relative to current sunk at IOVDD	I_{COMP_SINK}	RANGESEL1=0, output voltage = 100 mV	—	0.12	—	%
		RANGESEL1=1, output voltage = 100 mV	—	0.05	—	%
		RANGESEL1=2, output voltage = 150 mV	—	0.04	—	%
		RANGESEL1=3, output voltage = 250 mV	—	0.03	—	%

Note:

1. In IDAC_CURPROG register.
2. The IDAC is supplied by either AVDD, DVDD, or IOVDD based on the setting of ANASW in the EMU_PWRCTRL register and PWRSEL in the IDAC_CTRL register. Setting PWRSEL to 1 selects IOVDD. With PWRSEL cleared to 0, ANASW selects between AVDD (0) and DVDD (1).

4.1.17 Capacitive Sense (CSEN)

Table 4.25. Capacitive Sense (CSEN)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single conversion time (1x accumulation)	t_{CNV}	12-bit SAR Conversions	—	20.2	—	μs
		16-bit SAR Conversions	—	26.4	—	μs
		Delta Modulation Conversion (single comparison)	—	1.55	—	μs
Maximum external capacitive load	C_{EXTMAX}	CS0CG=7 (Gain = 1x), including routing parasitics	—	68	—	pF
		CS0CG=0 (Gain = 10x), including routing parasitics	—	680	—	pF
Maximum external series impedance	R_{EXTMAX}		—	1	—	kΩ
Supply current, EM2 bonded conversions, WARMUPMODE=NORMAL, WARMUPCNT=0	I_{CSEN_BOND}	12-bit SAR conversions, 20 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)[1]	—	326	—	nA
		Delta Modulation conversions, 20 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)[1]	—	226	—	nA
		12-bit SAR conversions, 200 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)[1]	—	33	—	nA
		Delta Modulation conversions, 200 ms conversion rate, CS0CG=7 (Gain = 1x), 10 channels bonded (total capacitance of 330 pF)[1]	—	25	—	nA
Supply current, EM2 scan conversions, WARMUPMODE=NORMAL, WARMUPCNT=0	I_{CSEN_EM2}	12-bit SAR conversions, 20 ms scan rate, CS0CG=0 (Gain = 10x), 8 samples per scan[1]	—	690	—	nA
		Delta Modulation conversions, 20 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), CS0CG=0 (Gain = 10x), 8 samples per scan[1]	—	515	—	nA
		12-bit SAR conversions, 200 ms scan rate, CS0CG=0 (Gain = 10x), 8 samples per scan[1]	—	79	—	nA
		Delta Modulation conversions, 200 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), CS0CG=0 (Gain = 10x), 8 samples per scan[1]	—	57	—	nA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current, continuous conversions, WARMUP-MODE=KEEPCSENWARM	I_{CSEN_ACTIVE}	SAR or Delta Modulation conversions of 33 pF capacitor, CS0CG=0 (Gain = 10x), always on	—	90.5	—	µA
HFPERCLK supply current	$I_{CSEN\_HFPERCLK}$	Current contribution from HFPERCLK when clock to CSEN block is enabled.	—	2.25	—	µA/MHz

Note:

1. Current is specified with a total external capacitance of 33 pF per channel. Average current is dependent on how long the module is actively sampling channels within the scan period, and scales with the number of samples acquired. Supply current for a specific application can be estimated by multiplying the current per sample by the total number of samples per period (total_current = single_sample_current * (number_of_channels * accumulation)).

4.1.18 Operational Amplifier (OPAMP)

Unless otherwise indicated, specified conditions are: Non-inverting input configuration, VDD = 3.3 V, DRIVESTRENGTH = 2, MAIN-OUTEN = 1, C_{LOAD} = 75 pF with OUTSCALE = 0, or C_{LOAD} = 37.5 pF with OUTSCALE = 1. Unit gain buffer and 3X-gain connection as specified in table footnotes[8] [1].

Table 4.26. Operational Amplifier (OPAMP)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply voltage	V_{OPA}	HCMDIS = 0, Rail-to-rail input range	2	—	3.8	V
		HCMDIS = 1	1.62	—	3.8	V
Input voltage	V_{IN}	HCMDIS = 0, Rail-to-rail input range	V_{VSS}	—	V_{OPA}	V
		HCMDIS = 1	V_{VSS}	—	V_{OPA}-1.2	V
Input impedance	R_{IN}		100	—	—	MΩ
Output voltage	V_{OUT}		V_{VSS}	—	V_{OPA}	V
Load capacitance[2]	C_{LOAD}	OUTSCALE = 0	—	—	75	pF
		OUTSCALE = 1	—	—	37.5	pF
Output impedance	R_{OUT}	DRIVESTRENGTH = 2 or 3, 0.4 V ≤ V_{OUT} ≤ V_{OPA} - 0.4 V, -8 mA < I_{OUT} < 8 mA, Buffer connection, Full supply range	—	0.25	—	Ω
		DRIVESTRENGTH = 0 or 1, 0.4 V ≤ V_{OUT} ≤ V_{OPA} - 0.4 V, -400 µA < I_{OUT} < 400 µA, Buffer connection, Full supply range	—	0.6	—	Ω
		DRIVESTRENGTH = 2 or 3, 0.1 V ≤ V_{OUT} ≤ V_{OPA} - 0.1 V, -2 mA < I_{OUT} < 2 mA, Buffer connection, Full supply range	—	0.4	—	Ω
		DRIVESTRENGTH = 0 or 1, 0.1 V ≤ V_{OUT} ≤ V_{OPA} - 0.1 V, -100 µA < I_{OUT} < 100 µA, Buffer connection, Full supply range	—	1	—	Ω
Internal closed-loop gain	G_{CL}	Buffer connection	TBD	1	TBD	-
		3x Gain connection	TBD	2.99	TBD	-
		16x Gain connection	TBD	15.7	TBD	-
Active current[4]	I_{OPA}	DRIVESTRENGTH = 3, OUT-SCALE = 0	—	580	—	µA
		DRIVESTRENGTH = 2, OUT-SCALE = 0	—	176	—	µA
		DRIVESTRENGTH = 1, OUT-SCALE = 0	—	13	—	µA
		DRIVESTRENGTH = 0, OUT-SCALE = 0	—	4.7	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Open-loop gain	G_{OL}	DRIVESTRENGTH = 3	—	135	—	dB
		DRIVESTRENGTH = 2	—	137	—	dB
		DRIVESTRENGTH = 1	—	121	—	dB
		DRIVESTRENGTH = 0	—	109	—	dB
Loop unit-gain frequency[7]	UGF	DRIVESTRENGTH = 3, Buffer connection	—	3.38	—	MHz
		DRIVESTRENGTH = 2, Buffer connection	—	0.9	—	MHz
		DRIVESTRENGTH = 1, Buffer connection	—	132	—	kHz
		DRIVESTRENGTH = 0, Buffer connection	—	34	—	kHz
		DRIVESTRENGTH = 3, 3x Gain connection	—	2.57	—	MHz
		DRIVESTRENGTH = 2, 3x Gain connection	—	0.71	—	MHz
		DRIVESTRENGTH = 1, 3x Gain connection	—	113	—	kHz
		DRIVESTRENGTH = 0, 3x Gain connection	—	28	—	kHz
Phase margin	PM	DRIVESTRENGTH = 3, Buffer connection	—	67	—	°
		DRIVESTRENGTH = 2, Buffer connection	—	69	—	°
		DRIVESTRENGTH = 1, Buffer connection	—	63	—	°
		DRIVESTRENGTH = 0, Buffer connection	—	68	—	°
Output voltage noise	N_{OUT}	DRIVESTRENGTH = 3, Buffer connection, 10 Hz - 10 MHz	—	146	—	µVrms
		DRIVESTRENGTH = 2, Buffer connection, 10 Hz - 10 MHz	—	163	—	µVrms
		DRIVESTRENGTH = 1, Buffer connection, 10 Hz - 1 MHz	—	170	—	µVrms
		DRIVESTRENGTH = 0, Buffer connection, 10 Hz - 1 MHz	—	176	—	µVrms
		DRIVESTRENGTH = 3, 3x Gain connection, 10 Hz - 10 MHz	—	313	—	µVrms
		DRIVESTRENGTH = 2, 3x Gain connection, 10 Hz - 10 MHz	—	271	—	µVrms
		DRIVESTRENGTH = 1, 3x Gain connection, 10 Hz - 1 MHz	—	247	—	µVrms
		DRIVESTRENGTH = 0, 3x Gain connection, 10 Hz - 1 MHz	—	245	—	µVrms

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Slew rate[5]	SR	DRIVESTRENGTH = 3, INCBW=1[3]	—	4.7	—	V/µs
		DRIVESTRENGTH = 3, INCBW=0	—	1.5	—	V/µs
		DRIVESTRENGTH = 2, INCBW=1[3]	—	1.27	—	V/µs
		DRIVESTRENGTH = 2, INCBW=0	—	0.42	—	V/µs
		DRIVESTRENGTH = 1, INCBW=1[3]	—	0.17	—	V/µs
		DRIVESTRENGTH = 1, INCBW=0	—	0.058	—	V/µs
		DRIVESTRENGTH = 0, INCBW=1[3]	—	0.044	—	V/µs
		DRIVESTRENGTH = 0, INCBW=0	—	0.015	—	V/µs
Startup time[6]	T_{START}	DRIVESTRENGTH = 2	—	—	TBD	µs
Input offset voltage	V_{OSI}	DRIVESTRENGTH = 2 or 3, T = 25 °C	TBD	—	TBD	mV
		DRIVESTRENGTH = 1 or 0, T = 25 °C	TBD	—	TBD	mV
		DRIVESTRENGTH = 2 or 3, across operating temperature range	TBD	—	TBD	mV
		DRIVESTRENGTH = 1 or 0, across operating temperature range	TBD	—	TBD	mV
DC power supply rejection ratio[9]	$PSRR_{DC}$	Input referred	—	70	—	dB
DC common-mode rejection ratio[9]	$CMRR_{DC}$	Input referred	—	70	—	dB
Total harmonic distortion	THD_{OPA}	DRIVESTRENGTH = 2, 3x Gain connection, 1 kHz, V_{OUT} = 0.1 V to V_{OPA} - 0.1 V	—	90	—	dB
		DRIVESTRENGTH = 0, 3x Gain connection, 0.1 kHz, V_{OUT} = 0.1 V to V_{OPA} - 0.1 V	—	90	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. Specified configuration for 3X-Gain configuration is: INCBW = 1, HCMDIS = 1, RESINSEL = VSS, V_{INPUT} = 0.5 V, V_{OUTPUT} = 1.5 V. Nominal voltage gain is 3.
2. If the maximum C_{LOAD} is exceeded, an isolation resistor is required for stability. See AN0038 for more information.
3. When INCBW is set to 1 the OPAMP bandwidth is increased. This is allowed only when the non-inverting close-loop gain is ≥ 3, or the OPAMP may not be stable.
4. Current into the load resistor is excluded. When the OPAMP is connected with closed-loop gain > 1, there will be extra current to drive the resistor feedback network. The internal resistor feedback network has total resistance of 143.5 kOhm, which will cause another ~10 µA current when the OPAMP drives 1.5 V between output and ground.
5. Step between 0.2V and V_{OPA}-0.2V, 10%-90% rising/falling range.
6. From enable to output settled. In sample-and-off mode, RC network after OPAMP will contribute extra delay. Settling error < 1mV.
7. In unit gain connection, UGF is the gain-bandwidth product of the OPAMP. In 3x Gain connection, UGF is the gain-bandwidth product of the OPAMP and 1/3 attenuation of the feedback network.
8. Specified configuration for Unit gain buffer configuration is: INCBW = 0, HCMDIS = 0, RESINSEL = DISABLE. V_{INPUT} = 0.5 V, V_{OUTPUT} = 0.5 V.
9. When HCMDIS=1 and input common mode transitions the region from V_{OPA}-1.4V to V_{OPA}-1V, input offset will change. PSRR and CMRR specifications do not apply to this transition region.

4.1.19 LCD Driver

Table 4.27. LCD Driver

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frame rate	f_{LCDFR}		TBD	—	TBD	Hz
LCD supply voltage range	V_{LCD}		2.0	—	3.8	V
Current consumption, constant display	I_{LCD}	Current source mode, No external LCD capacitor, AVDD = 3.3 V, VLCD < AVDD - 400 mV, 40 segments x 1 common, frame rate = 60 Hz, Bias = TBD	—	TBD	—	µA
		Step-down mode with external LCD capacitor, AVDD = 3.3 V, VLCD = 3.0 V, 40 segments x 4 commons, frame rate = 60 Hz, Bias = TBD	—	TBD	—	µA
		Charge pump mode with external LCD capacitor, AVDD = 2.7, VLCD = 3.0 V, 40 segments x 4 commons, frame rate = 60 Hz, Bias = TBD	—	TBD	—	µA
Contrast control accuracy	$ACC_{CONTRAST}$		—	TBD	—	%

4.1.20 Pulse Counter (PCNT)

Table 4.28. Pulse Counter (PCNT)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input frequency	F_{IN}	Asynchronous Single and Quadrature Modes	—	—	20	MHz
		Sampled Modes with Debounce filter set to 0.	—	—	8	kHz

4.1.21 Analog Port (APORT)

Table 4.29. Analog Port (APORT)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current[2] [1]	I_{APORT}	Operation in EM0/EM1	—	7	—	μA
		Operation in EM2/EM3	—	915	—	nA

Note:

1. Specified current is for continuous APORT operation. In applications where the APORT is not requested continuously (e.g. periodic ACMP requests from LESENSE in EM2), the average current requirements can be estimated by mutiplying the duty cycle of the requests by the specified continuous current number.
2. Supply current increase that occurs when an analog peripheral requests access to APORT. This current is not included in reported module currents. Additional peripherals requesting access to APORT do not incur further current.

4.1.22 I2C

4.1.22.1 I2C Standard-mode (Sm)[1]

Table 4.30. I2C Standard-mode (Sm)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	100	kHz
SCL clock low time	t_{LOW}		4.7	—	—	µs
SCL clock high time	t_{HIGH}		4	—	—	µs
SDA set-up time	t_{SU_DAT}		250	—	—	ns
SDA hold time[3]	t_{HD_DAT}		100	—	3450	ns
Repeated START condition set-up time	t_{SU_STA}		4.7	—	—	µs
(Repeated) START condition hold time	t_{HD_STA}		4	—	—	µs
STOP condition set-up time	t_{SU_STO}		4	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		4.7	—	—	µs

Note:

1. For CLHR set to 0 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Standard-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time (t_{HD_DAT}) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

4.1.22.2 I2C Fast-mode (Fm)[1]

Table 4.31. I2C Fast-mode (Fm)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	400	kHz
SCL clock low time	t_{LOW}		1.3	—	—	µs
SCL clock high time	t_{HIGH}		0.6	—	—	µs
SDA set-up time	t_{SU_DAT}		100	—	—	ns
SDA hold time[3]	t_{HD_DAT}		100	—	900	ns
Repeated START condition set-up time	t_{SU_STA}		0.6	—	—	µs
(Repeated) START condition hold time	t_{HD_STA}		0.6	—	—	µs
STOP condition set-up time	t_{SU_STO}		0.6	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		1.3	—	—	µs

Note:
1. For CLHR set to 1 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Fast-mode, refer to the I2C chapter in the reference manual.
3. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).

4.1.22.3 I2C Fast-mode Plus (Fm+)[1]

Table 4.32. I2C Fast-mode Plus (Fm+)[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency[2]	f_{SCL}		0	—	1000	kHz
SCL clock low time	t_{LOW}		0.5	—	—	µs
SCL clock high time	t_{HIGH}		0.26	—	—	µs
SDA set-up time	t_{SU_DAT}		50	—	—	ns
SDA hold time	t_{HD_DAT}		100	—	—	ns
Repeated START condition set-up time	t_{SU_STA}		0.26	—	—	µs
(Repeated) START condition hold time	t_{HD_STA}		0.26	—	—	µs
STOP condition set-up time	t_{SU_STO}		0.26	—	—	µs
Bus free time between a STOP and START condition	t_{BUF}		0.5	—	—	µs

Note:

1. For CLHR set to 0 or 1 in the I2Cn_CTRL register.
2. For the minimum HFPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual.

4.1.23 USART SPI

SPI Master Timing

Table 4.33. SPI Master Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1 3 2]	t_{SCLK}	All USARTs except USART2	2 * $t_{HFPERCLK}$	—	—	ns
		USART2	2 * $t_{HFPERBCLK}$	—	—	ns
CS to MOSI [1 3]	t_{CS_MO}	USART2, location 4, IOVDD = 1.8 V	-3.2	—	6.8	ns
		USART2, location 4, IOVDD = 3.0 V	-2.3	—	6.0	ns
		USART2, location 5, IOVDD = 1.8 V	-8.1	—	6.3	ns
		USART2, location 5, IOVDD = 3.0 V	-7.3	—	4.4	ns
		All other USARTs and locations, IOVDD = 1.8 V	-14.3	—	11.3	ns
		All other USARTs and locations, IOVDD = 3.0 V	-12.4	—	9.0	ns
SCLK to MOSI [1 3]	t_{SCLK_MO}	USART2, location 4, IOVDD = 1.8 V	-0.3	—	9.2	ns
		USART2, location 4, IOVDD = 3.0 V	-0.3	—	8.6	ns
		USART2, location 5, IOVDD = 1.8 V	-3.6	—	5.0	ns
		USART2, location 5, IOVDD = 3.0 V	-3.4	—	3.2	ns
		All other USARTs and locations, IOVDD = 1.8 V	-9.7	—	10.3	ns
		All other USARTs and locations, IOVDD = 3.0 V	-8.4	—	10.7	ns
MISO setup time [1 3]	t_{SU_MI}	USART2, location 4, IOVDD = 1.8 V	39.7	—	—	ns
		USART2, location 4, IOVDD = 3.0 V	22.4	—	—	ns
		USART2, location 5, IOVDD = 1.8 V	49.2	—	—	ns
		USART2, location 5, IOVDD = 3.0 V	30.0	—	—	ns
		All other USARTs and locations, IOVDD = 1.8 V	45.5	—	—	ns
		All other USARTs and locations, IOVDD = 3.0 V	34.4	—	—	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
MISO hold time [1] [3]	t_{H_MI}	USART2, location 4, IOVDD = 1.8 V	-11.6	—	—	ns
		USART2, location 4, IOVDD = 3.0 V	-11.6	—	—	ns
		USART2, location 5, IOVDD = 1.8 V	-9.1	—	—	ns
		USART2, location 5, IOVDD = 3.0 V	-9.1	—	—	ns
		All other USARTs and locations, IOVDD = 1.8 V	-7.9	—	—	ns
		All other USARTs and locations, IOVDD = 3.0 V	-7.9	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

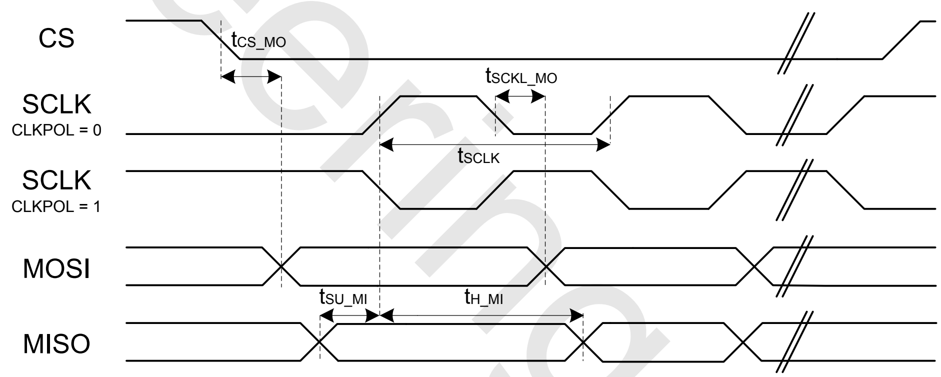


Figure 4.1. SPI Master Timing Diagram

SPI Slave Timing

Table 4.34. SPI Slave Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1 3 2]	t_{SCLK}		6 * $t_{HFPERCLK}$	—	—	ns
SCLK high time[1 3 2]	t_{SCLK_HI}		2.5 * $t_{HFPERCLK}$	—	—	ns
SCLK low time[1 3 2]	t_{SCLK_LO}		2.5 * $t_{HFPERCLK}$	—	—	ns
CS active to MISO [1 3]	$t_{CS\_ACT\_MI}$		20	—	70	ns
CS disable to MISO [1 3]	$t_{CS\_DIS\_MI}$		15	—	135	ns
MOSI setup time [1 3]	t_{SU_MO}		4	—	—	ns
MOSI hold time [1 3 2]	t_{H_MO}		7	—	—	ns
SCLK to MISO [1 3 2]	t_{SCLK_MI}		15 + 1.5 * $t_{HFPERCLK}$	—	45 + 2.5 * $t_{HFPERCLK}$	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

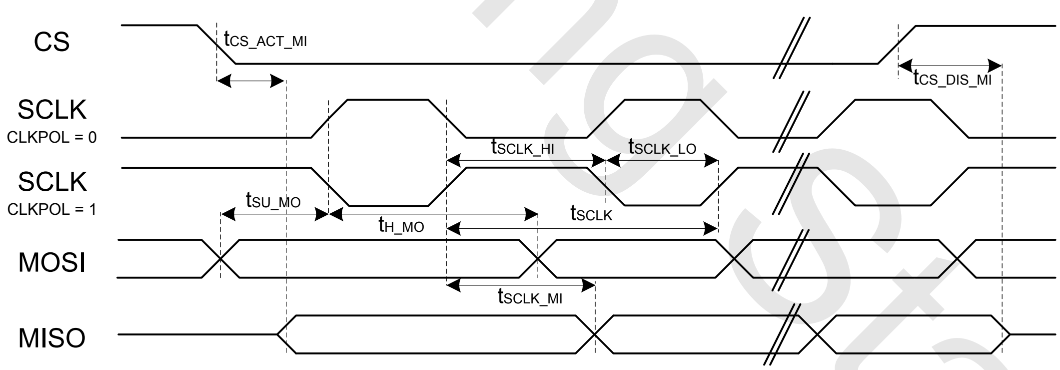


Figure 4.2. SPI Slave Timing Diagram

4.1.24 External Bus Interface (EBI)

EBI Write Enable Output Timing

Timing applies to both EBI_WEn and EBI_NANDWEn for all addressing modes and both polarities. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.35. EBI Write Enable Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output hold time, from trailing EBI_WEn / EBI_NANDWEn edge to EBI_AD, EBI_A, EBI_CSn, EBI_BLn invalid	t_{OH_WEn}	IOVDD ≥ 1.62 V	-21.66 + (WRHOLD * $t\{_{\}HFCORECLK\{}\}$)	—	—	ns
		IOVDD ≥ 3.0 V	-12.24 + (WRHOLD * $t_{HFCORECLK}$)	—	—	ns
Output setup time, from EBI_AD, EBI_A, EBI_CSn, EBI_BLn valid to leading EBI_WEn / EBI_NANDWEn edge[1]	t_{OSU_WEn}	IOVDD ≥ 1.62 V	-11.12 + (WRSETUP * $t_{HFCORECLK}$)	—	—	ns
		IOVDD ≥ 3.0 V	-9.52 + (WRSETUP * $t_{HFCORECLK}$)	—	—	ns
EBI_WEn / EBI_NANDWEn pulse width[1]	t_{WIDTH_WEn}	IOVDD ≥ 1.62 V	-5.81 + ((WRSTRB + 1) * $t_{HFCORECLK}$)	—	—	ns
		IOVDD ≥ 3.0 V	-4.04 + ((WRSTRB + 1) * $t_{HFCORECLK}$)	—	—	ns

Note:

1. The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFWE=0. The leading edge of EBI_WEn can be moved to the right by setting HALFWE=1. This decreases the length of t_{WIDTH_WEn} and increases the length of t_{OSU_WEn} by 1/2 * $t_{HFCLKNODIV}$.

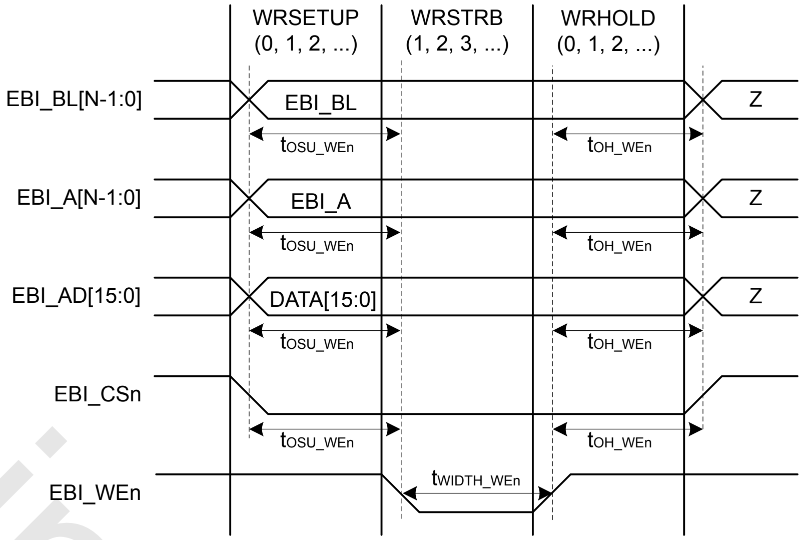


Figure 4.3. EBI Write Enable Output Timing Diagram

EBI Address Latch Enable Output Timing

Timing applies to multiplexed addressing modes D8A24ALE and D16A16ALE for both polarities. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.36. EBI Address Latch Enable Output Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output hold time, from trailing EBI_ALE edge to EBI_AD invalid[1 2]	t_{OH_ALEn}	IOVDD ≥ 1.62 V	-21.68 + (ADDRHOLD * $t_{HFCORECLK}$)	—	—	ns
		IOVDD ≥ 3.0 V	-10.93 + (ADDRHOLD * $t_{HFCORECLK}$)	—	—	ns
Output setup time, from EBI_AD valid to leading EBI_ALE edge	t_{OSU_ALEn}	IOVDD ≥ 1.62 V	-11.25	—	—	ns
		IOVDD ≥ 3.0 V	-8.63	—	—	ns
EBI_ALEn pulse width[1]	t_{WIDTH_ALEn}	IOVDD ≥ 1.62 V	-3.94 + ((ADDRSETUP + 1) * t{}HFCORECLK{})	—	—	ns
		IOVDD ≥ 3.0 V	-2.57 + ((ADDRSETUP + 1) * t{}HFCORECLK{})	—	—	ns

Note:

1. The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFALE=0. The trailing edge of EBI_ALEn can be moved to the left by setting HALFALE=1. This decreases the length of t_{WIDTH_ALEn} and increases the length of t_{OSU_ALEn} by $t_{HFCORECLK}$ - 1/2 * $t_{HFCLKNODIV}$.
2. The figure shows a write operation. For a multiplexed read operation the address hold time is controlled via the RDSETUP state instead of via the ADDRHOLD state.

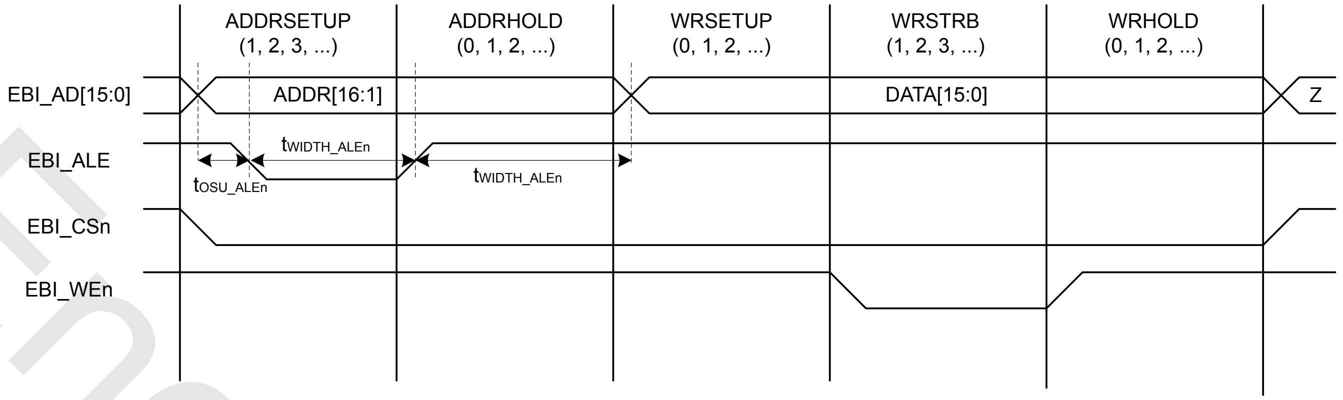


Figure 4.4. EBI Address Latch Enable Output Timing Diagram

EBI Read Enable Output Timing

Timing applies to both EBI_REn and EBI_NANDREn for all addressing modes and both polarities. Output timing for EBI_AD applies only to multiplexed addressing modes D8A24ALE and D16A16ALE. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.37. EBI Read Enable Output Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output hold time, from trailing EBI_REn / EBI_NANDREn edge to EBI_AD, EBI_A, EBI_CSn, EBI_BLn invalid	t_{OH_REn}	IOVDD ≥ 1.62 V	-22.70 + (RDHOLD * $t_{HFCORECLK}$)	—	—	ns
		IOVDD ≥ 3.0 V	-12.60 + (RDHOLD * $t_{HFCORECLK}$)	—	—	ns
Output setup time, from EBI_AD, EBI_A, EBI_CSn, EBI_BLn valid to leading EBI_REn / EBI_NANDREn edge [1]	t_{OSU_REn}	IOVDD ≥ 1.62 V	-11.49 + (RDSETUP * $t_{HFCORECLK}$)	—	—	ns
		IOVDD ≥ 3.0 V	-10.04 + (RDSETUP * $t_{HFCORECLK}$)	—	—	ns
EBI_REn pulse width[1] [2]	t_{WIDTH_REn}	IOVDD ≥ 1.62 V	-5.34 + ((RDSTRB + 1) * $t_{HFCORECLK}$)	—	—	ns
		IOVDD ≥ 3.0 V	-3.21 + ((RDSTRB + 1) * $t_{HFCORECLK}$)	—	—	ns

Note:

1. The figure shows the timing for the case that the half strobe length functionality is not used, i.e. HALFRE=0. The leading edge of EBI_REn can be moved to the right by setting HALFRE=1. This decreases the length of t_{WIDTH_REn} and increases the length of t_{OSU_REn} by 1/2 * $t_{HFCLKNODIV}$.
2. When page mode is used, RDSTRB is replaced by RDPA for page hits.

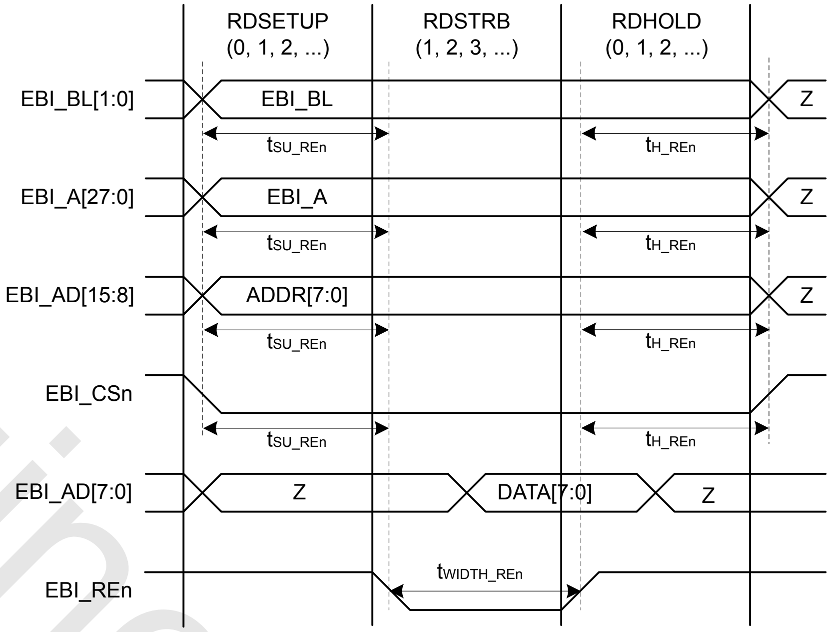


Figure 4.5. EBI Read Enable Output Timing Diagram

EBI TFT Output Timing

All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.38. EBI TFT Output Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output hold time, EBI_DCLK to EBI_AD invalid	t_{OH_DCLK}	IOVDD ≥ 1.62 V	-22.38 + (TFTHOLD * $t_{HFCORECLK}$)	—	—	ns
		IOVDD ≥ 3.0 V	-11.40 + (TFTHOLD * $t_{HFCORECLK}$)	—	—	ns
Output setup time, EBI_AD valid to EBI_DCLK	t_{OSU_DCLK}	IOVDD ≥ 1.62 V	-10.96 + (TFTSETUP * $t_{HFCORECLK}$)	—	—	ns
		IOVDD ≥ 3.0 V	-8.63 + (TFTSETUP * $t_{HFCORECLK}$)	—	—	ns

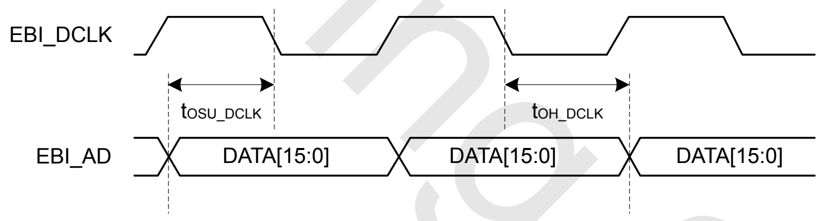


Figure 4.6. EBI TFT Output Timing

EBI Read Enable Timing Requirements

Timing applies to both EBI_REn and EBI_NANDREn for all addressing modes and both polarities. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.39. EBI Read Enable Timing Requirements

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Setup time, from EBI_AD valid to trailing EBI_REn edge	t_{SU_REn}	IOVDD ≥ 1.62 V	54.66	—	—	ns
		IOVDD ≥ 3.0 V	35.20	—	—	ns
Hold time, from trailing EBI_REn edge to EBI_AD invalid	t_{H_REn}	IOVDD ≥ 1.62 V	-9.80	—	—	ns

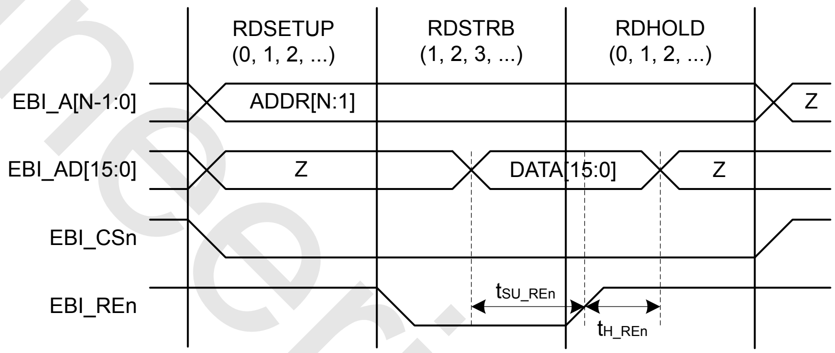


Figure 4.7. EBI Read Enable Timing Requirements

EBI Ready/Wait Timing Requirements

Timing applies to both EBI_REn and EBI_WEn for all addressing modes and both polarities. All numbers are based on route locations 0,1,2 only (with all EBI alternate functions using the same location at the same time). Timing is specified at 10% and 90% of IOVDD, 25 pF external loading, and slew rate for all GPIO set to 6.

Table 4.40. EBI Ready/Wait Timing Requirements

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Setup time, from EBI_ARDY valid to trailing EBI_REn, EBI_WEn edge	t_{SU_ARDY}	IOVDD ≥ 1.62 V	54.42 + (3 * $t_{HFCORECLK}$)	—	—	ns
		IOVDD ≥ 3.0 V	35.47 + (3 * $t_{HFCORECLK}$)	—	—	ns
Hold time, from trailing EBI_REn, EBI_WEn edge to EBI_ARDY invalid	t_{H_ARDY}	IOVDD ≥ 1.62 V	-10.18	—	—	ns

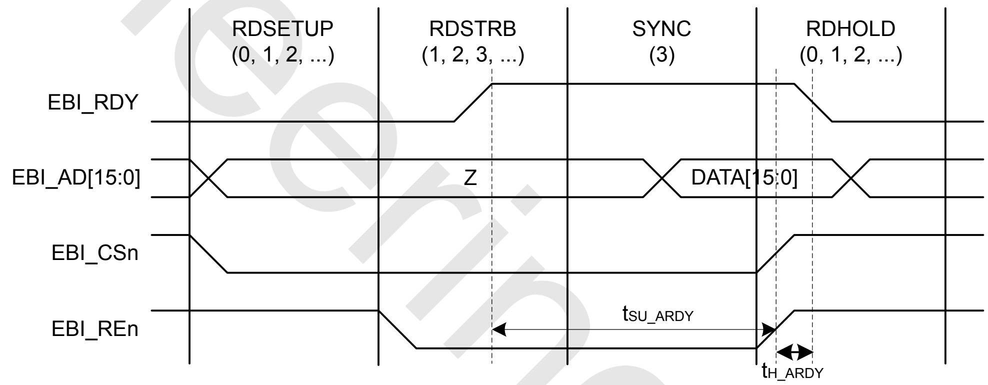


Figure 4.8. EBI Ready/Wait Timing Requirements

4.1.25 Ethernet (ETH)

MII Transmit Timing

Timing is specified with 3.0 V ≤ IOVDD ≤ 3.8 V, 25 pF external loading, and slew rate for all GPIO set to 6 unless otherwise indicated.

Table 4.41. Ethernet MII Transmit Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TX_CLK frequency	F_{TX_CLK}	Output slew rate set to 7	—	25	—	MHz
TX_CLK duty cycle	DC_{TX_CLK}		35	—	65	%
Output delay, TX_CLK to TXD[3:0], TX_EN, TX_ER	t_{OUT}		0	—	25	ns

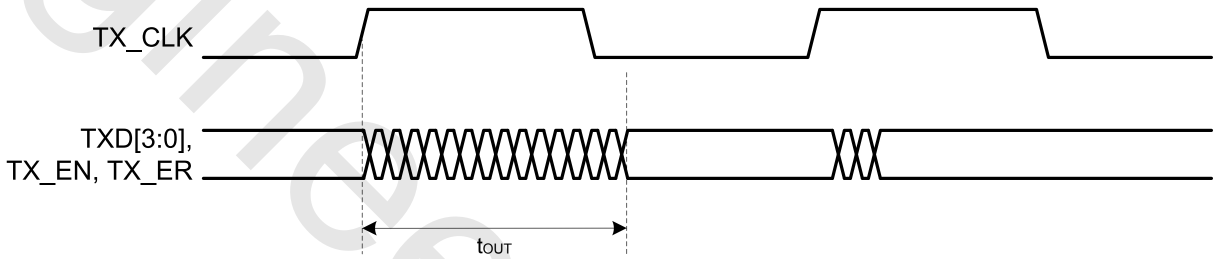


Figure 4.9. Ethernet MII Transmit Timing

MII Receive Timing

Timing is specified with 3.0 V ≤ IOVDD ≤ 3.8 V, 25 pF external loading, and slew rate for all GPIO set to 6 unless otherwise indicated.

Table 4.42. Ethernet MII Receive Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RX_CLK frequency	F_{RX_CLK}		—	25	—	MHz
RX_CLK duty cycle	DC_{RX_CLK}		35	—	65	%
Setup time, RXD[3:0], RX_DV, RX_ER valid to RX_CLK	t_{SU}		6	—	—	ns
Hold time, RX_CLK to RXD[3:0], RX_DV, RX_ER change	t_{HD}		5	—	—	ns

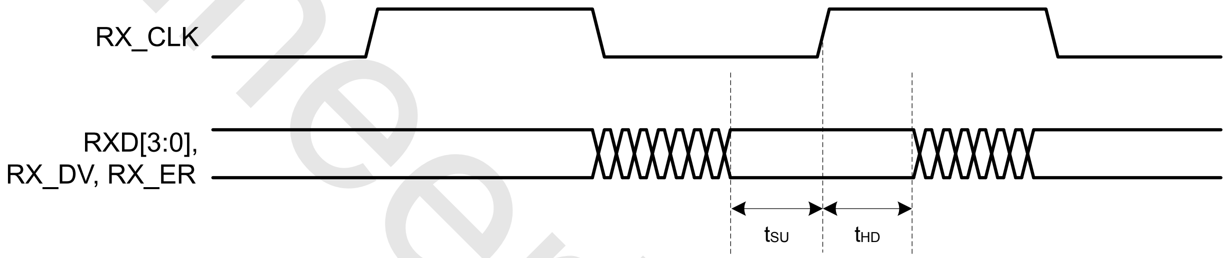


Figure 4.10. Ethernet MII Receive Timing

RMII Transmit Timing

Timing is specified with 3.0 V ≤ IOVDD ≤ 3.8 V, 25 pF external loading, and slew rate for all GPIO set to 6 unless otherwise indicated.

Table 4.43. Ethernet RMII Transmit Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
REF_CLK frequency	F_{REF_CLK}	Output slew rate set to 7	—	50	—	MHz
REF_CLK duty cycle	DC_{REF_CLK}		35	—	65	%
Output delay, REF_CLK to TXD[1:0], TX_EN	t_{OUT}		2.3	—	14.1	ns

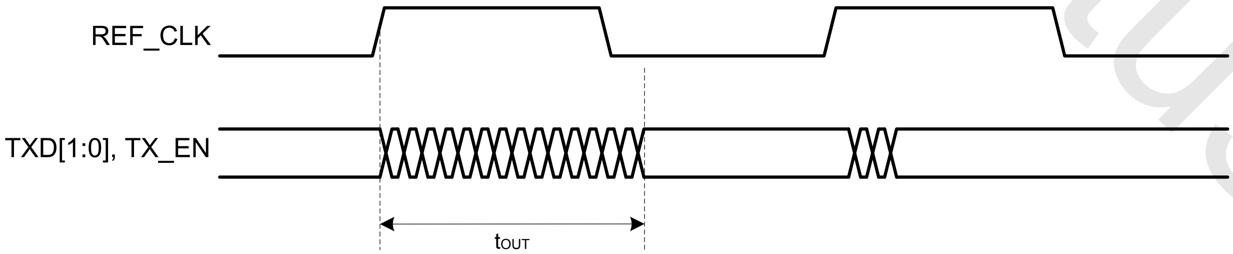


Figure 4.11. Ethernet RMII Transmit Timing

RMII Receive Timing

Timing is specified with 3.0 V ≤ IOVDD ≤ 3.8 V, 25 pF external loading, and slew rate for all GPIO set to 6 unless otherwise indicated.

Table 4.44. Ethernet RMII Receive Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
REF_CLK frequency	F_{REF_CLK}	Output slew rate set to 7	—	50	—	MHz
REF_CLK duty cycle	DC_{REF_CLK}		35	—	65	%
Setup time, RXD[1:0], CRS_DV, RX_ER valid to REF_CLK	t_{SU}		4	—	—	ns
Hold time, REF_CLK to RXD[1:0], CRS_DV, RX_ER change	t_{HD}		2	—	—	ns

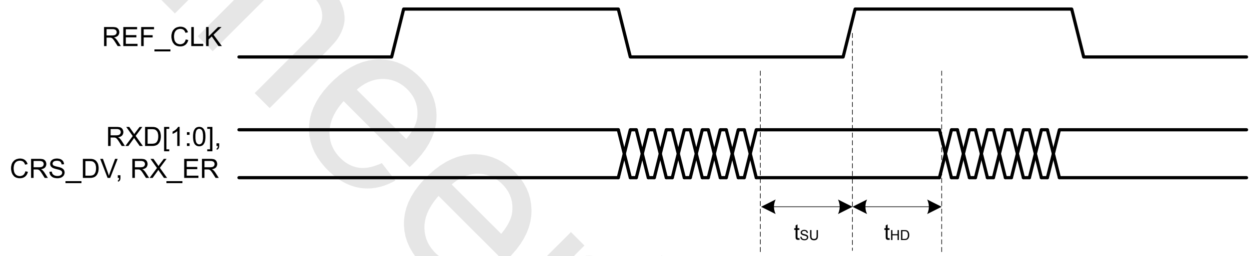


Figure 4.12. Ethernet RMII Receive Timing

4.1.26 Serial Data I/O Host Controller (SDIO)

SDIO DS Mode Timing

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled and slew rate for all GPIO set to 6.

Table 4.45. SDIO DS Mode Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	$C_L \leq 10$ pF	0	—	25	MHz
Clock low time	t_{WL}	$C_L \leq 10$ pF	18	—	20	ns
Clock high time	t_{WH}	$C_L \leq 10$ pF	18	—	20	ns
Clock rise time	t_R	$C_L \leq 10$ pF	1.69	3.23	—	ns
Clock fall time	t_F	$C_L \leq 10$ pF	1.42	2.79	—	ns
Input setup time, CMD, DAT[0:3] valid to SD_CLK	t_{ISU}	$C_L \leq 10$ pF	6	—	—	ns
Input hold time, SD_CLK to CMD, DAT[0:3] change	t_{IH}	$C_L \leq 10$ pF	0	—	—	ns
Output delay time, SD_CLK to CMD, DAT[0:3] valid	t_{ODLY}	$C_L \leq 40$ pF	0	—	14	ns
Output hold time, SD_CLK to CMD, DAT[0:3] change	t_{OH}	$C_L \leq 40$ pF	5	—	—	ns

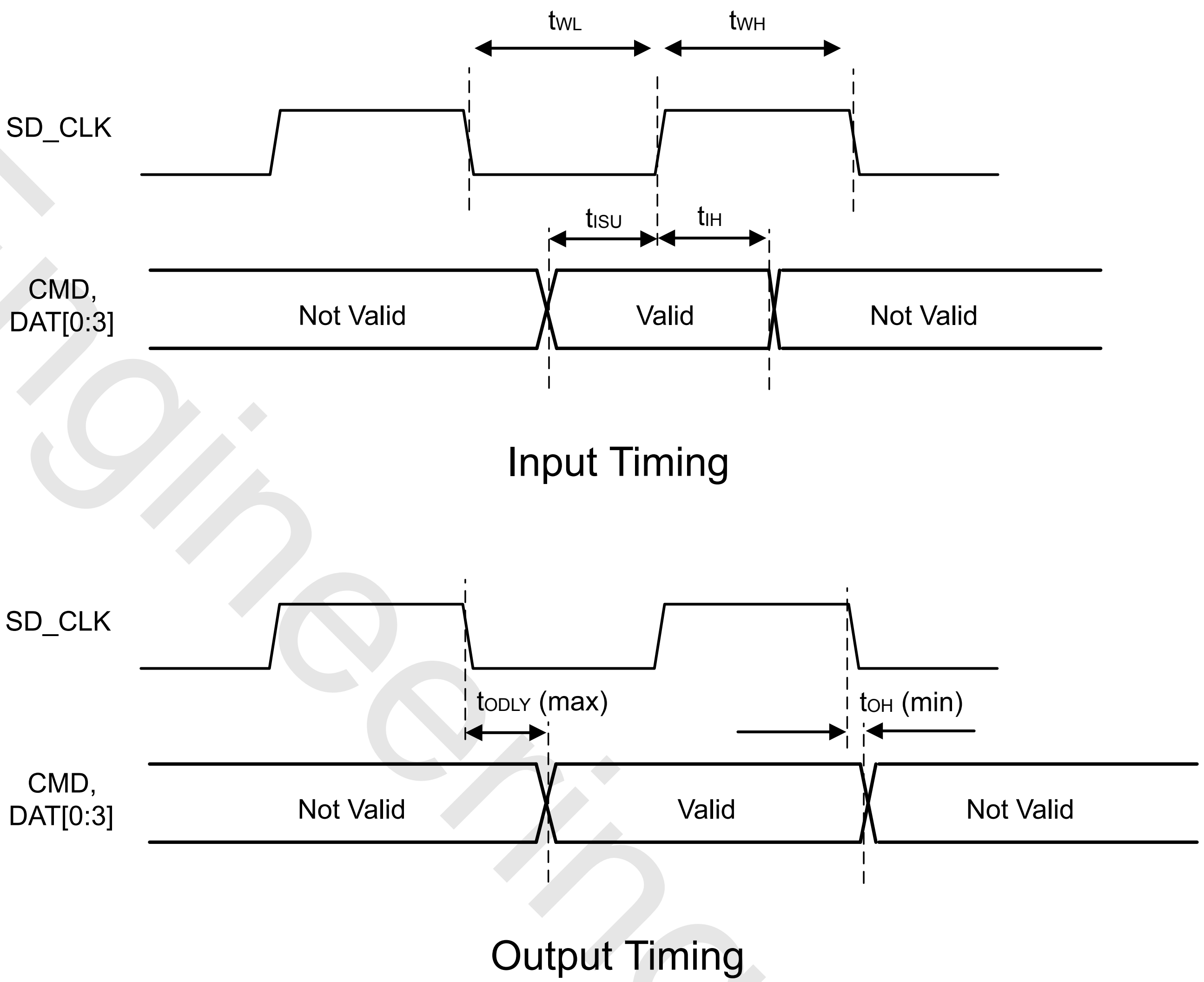


Figure 4.13. SDIO DS Mode Timing

SDIO HS Mode Timing

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled and slew rate for all GPIO set to 6.

Table 4.46. SDIO HS Mode Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	$C_L \leq 10$ pF	0	—	50	MHz
Clock low time	t_{WL}	$C_L \leq 10$ pF	9	—	10	ns
Clock high time	t_{WH}	$C_L \leq 10$ pF	9	—	10	ns
Clock rise time	t_R	$C_L \leq 10$ pF	1.69	3.23	—	ns
Clock fall time	t_F	$C_L \leq 10$ pF	1.42	2.79	—	ns
Input setup time, CMD, DAT[0:3] valid to SD_CLK	t_{ISU}	$C_L \leq 10$ pF	6	—	—	ns
Input hold time, SD_CLK to CMD, DAT[0:3] change	t_{IH}	$C_L \leq 10$ pF	2.5	—	—	ns
Output delay time, SD_CLK to CMD, DAT[0:3] valid	t_{ODLY}	$C_L \leq 25$ pF	0	—	13	ns
Output hold time, SD_CLK to CMD, DAT[0:3] change	t_{OH}	$C_L \leq 25$ pF	2	—	—	ns

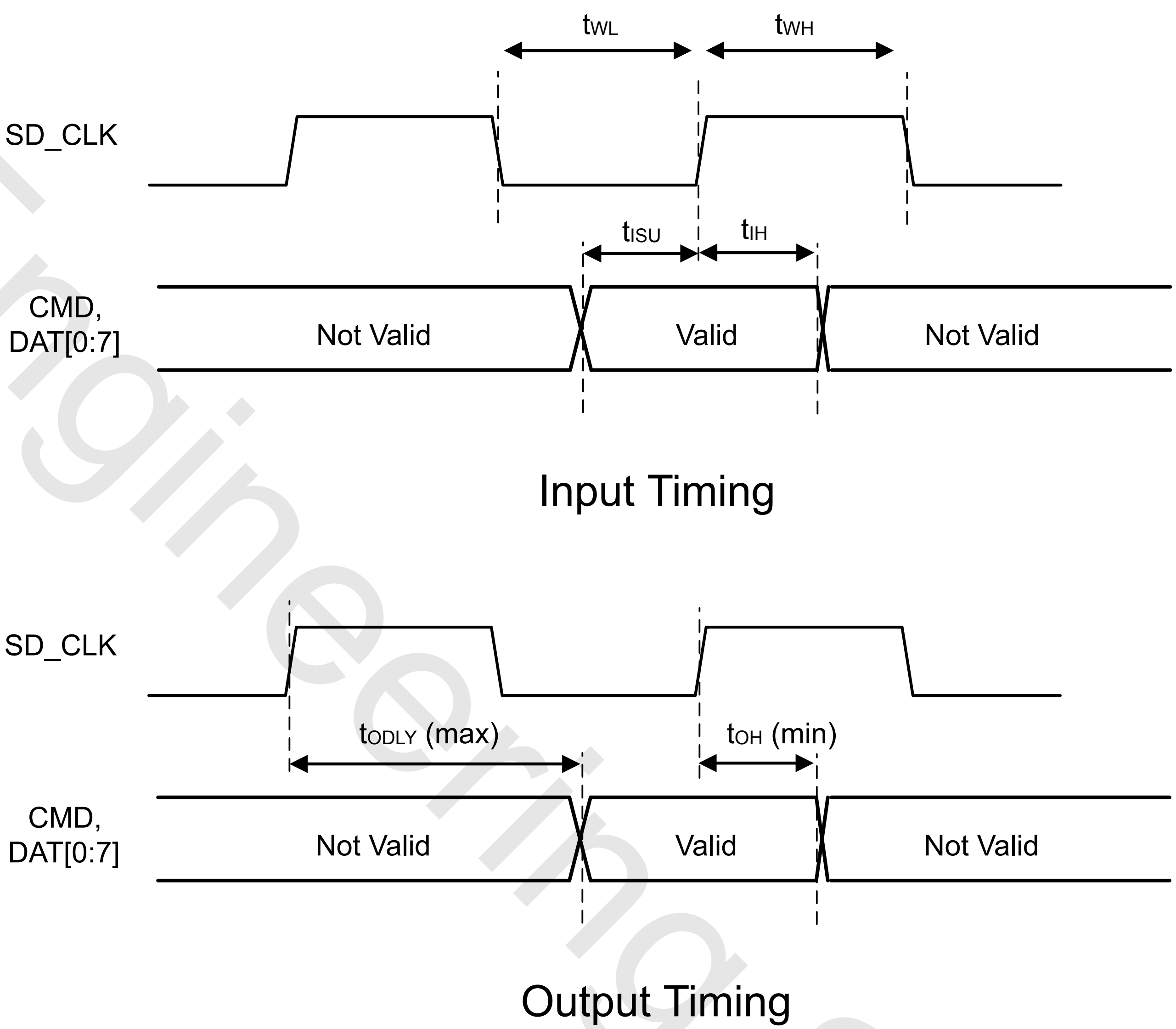


Figure 4.14. SDIO HS Mode Timing

SDIO SDR Mode Timing

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled and slew rate for SD_CLK set to 7, all other GPIO set to 6.

Table 4.47. SDIO SDR Mode Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	Loading on SD_CLK = 10 pF	0	—	25	MHz
Clock low time	t_{WL}	Loading on SD_CLK = 10 pF	18	—	20	ns
Clock high time	t_{WH}	Loading on SD_CLK = 10 pF	18	—	20	ns
Clock rise time	t_R	Loading on SD_CLK = 10 pF	0.99	4.68	—	ns
Clock fall time	t_F	Loading on SD_CLK = 10 pF	0.90	3.64	—	ns
Input setup time, CMD, DAT[0:3] valid to SD_CLK	t_{ISU}	Loading on CMD, DAT[0:3] = 10 pF	6	—	—	ns
Input hold time, SD_CLK to CMD, DAT[0:3] change	t_{IH}	Loading on CMD, DAT[0:3] = 5 pF	1.5	—	—	ns
Output delay time, SD_CLK to CMD, DAT[0:3] valid	t_{ODLY}	Loading on CMD, DAT[0:3] = 40 pF	0	—	35	ns
Output hold time, SD_CLK to CMD, DAT[0:3] change	t_{OH}	Loading on CMD, DAT[0:3] = 40 pF	0.8	—	—	ns

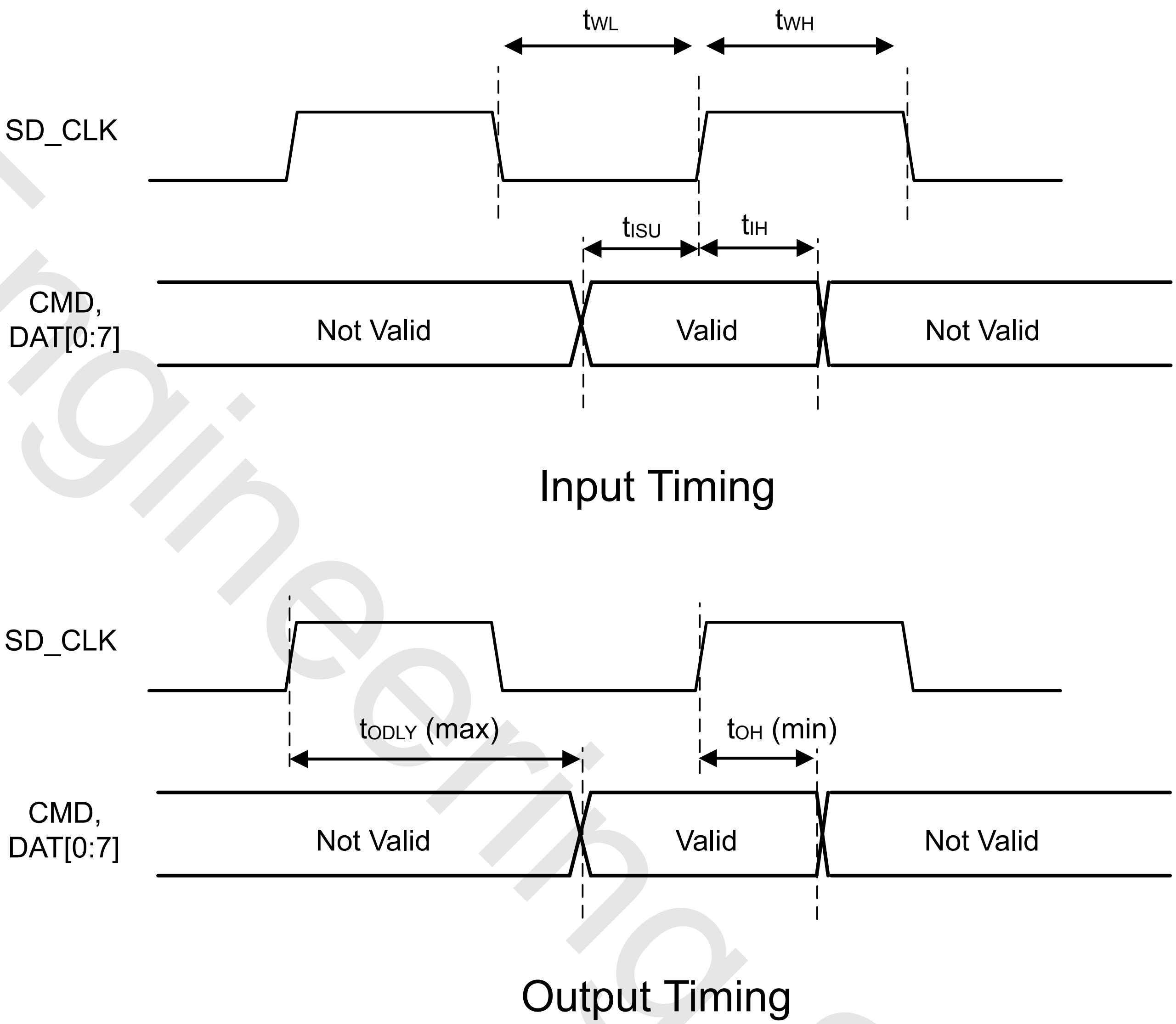


Figure 4.15. SDIO SDR Mode Timing

SDIO DDR Mode Timing

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled and slew rate for all GPIO set to 6.

Table 4.48. SDIO DDR Mode Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	$C_L \leq 10$ pF	0	—	25	MHz
Clock low time	t_{WL}	$C_L \leq 10$ pF	18	—	20	ns
Clock high time	t_{WH}	$C_L \leq 10$ pF	18	—	20	ns
Clock rise time	t_R	$C_L \leq 10$ pF	1.69	6.52	—	ns
Clock fall time	t_F	$C_L \leq 10$ pF	1.42	4.96	—	ns
Input setup time, CMD valid to SD_CLK	t_{ISU}	$C_L \leq 10$ pF	6	—	—	ns
Input hold time, SD_CLK to CMD change	t_{IH}	$C_L \leq 10$ pF	1.8	—	—	ns
Output delay time, SD_CLK to CMD valid	t_{ODLY}	$C_L \leq 30$ pF	0	—	16	ns
Output hold time, SD_CLK to CMD change	t_{OH}	$C_L \leq 15$ pF	0.8	—	—	ns
Input setup time, DAT[0:3] valid to SD_CLK	t_{ISU2X}	$C_L \leq 10$ pF	6	—	—	ns
Input hold time, SD_CLK to DAT[0:3] change	t_{IH2X}	$C_L \leq 10$ pF	1.5	—	—	ns
Output delay time, SD_CLK to DAT[0:3] valid	t_{ODLY2X}	$C_L \leq 25$ pF	0	—	16	ns
Output hold time, SD_CLK to DAT[0:3] change	t_{OH2X}	$C_L \leq 15$ pF	0.8	—	—	ns

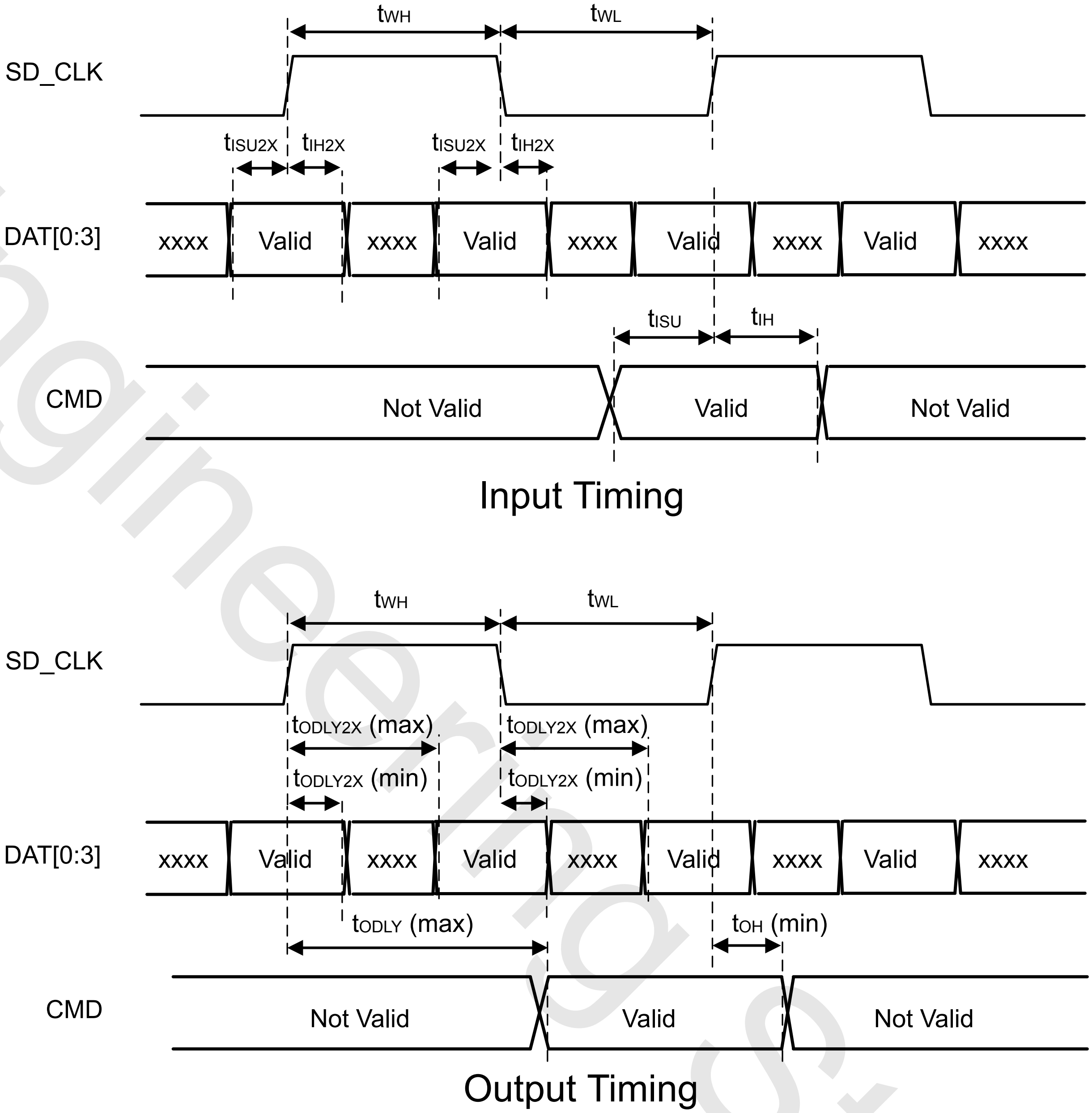


Figure 4.16. SDIO DDR Mode Timing

SDIO MMC Legacy Mode Timing

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled and slew rate for SD_CLK set to 7, all other GPIO set to 6.

Table 4.49. SDIO MMC Legacy Mode Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	$C_L \leq 30$ pF	0	—	25	MHz
Clock low time	t_{WL}	$C_L \leq 30$ pF	18	—	20	ns
Clock high time	t_{WH}	$C_L \leq 30$ pF	18	—	20	ns
Clock rise time	t_R	$C_L \leq 30$ pF	1.96	3.87	—	ns
Clock fall time	t_F	$C_L \leq 30$ pF	1.67	3.31	—	ns
Input setup time, CMD, DAT[0:7] valid to SD_CLK	t_{ISU}	$C_L \leq 30$ pF	8	—	—	ns
Input hold time, SD_CLK to CMD, DAT[0:3] change	t_{IH}	$C_L \leq 30$ pF	8.3	—	—	ns
Output delay time, SD_CLK to CMD, DAT[0:7] valid	t_{ODLY}	$C_L \leq 30$ pF	0	—	36	ns
Output hold time, SD_CLK to CMD, DAT[0:7] change	t_{OH}	$C_L \leq 30$ pF	3	—	—	ns

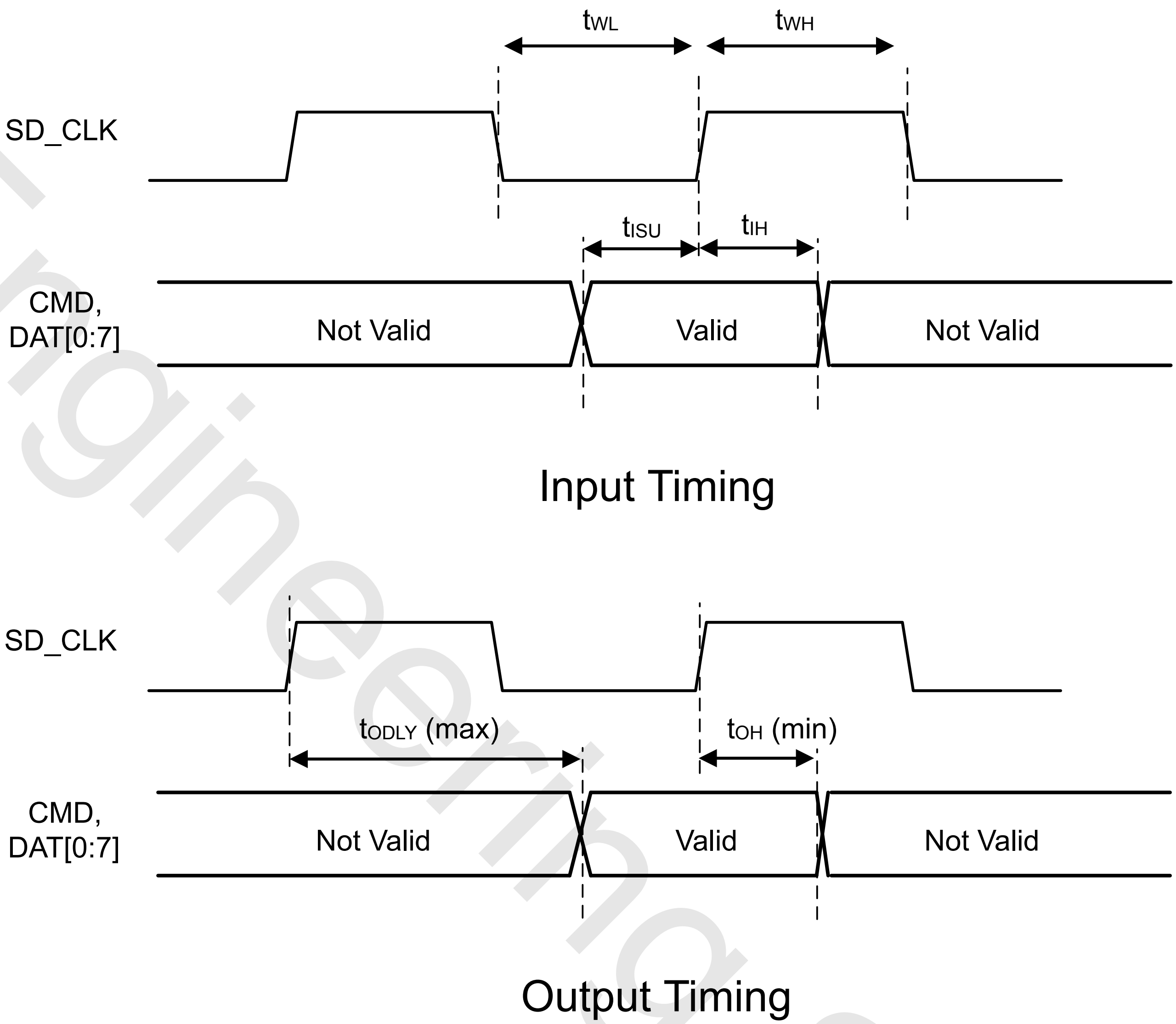


Figure 4.17. SDIO MMC Legacy Mode Timing

SDIO MMC SDR Mode Timing at 1.8 V

Timing is specified for route location 0 at 1.8 V IOVDD with voltage scaling disabled and slew rate for SD_CLK set to 7, all other GPIO set to 6.

Table 4.50. SDIO MMC SDR Mode 1.8V Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	$C_L \leq 30$ pF	0	—	25	MHz
Clock low time	t_{WL}	$C_L \leq 30$ pF	18	—	20	ns
Clock high time	t_{WH}	$C_L \leq 30$ pF	18	—	20	ns
Clock rise time	t_R	$C_L \leq 30$ pF	1.96	8.27	—	ns
Clock fall time	t_F	$C_L \leq 30$ pF	1.67	6.90	—	ns
Input setup time, CMD, DAT[0:7] valid to SD_CLK	t_{ISU}	$C_L \leq 30$ pF	5.3	—	—	ns
Input hold time, SD_CLK to CMD, DAT[0:3] change	t_{IH}	$C_L \leq 30$ pF	2.5	—	—	ns
Output delay time, SD_CLK to CMD, DAT[0:7] valid	t_{ODLY}	$C_L \leq 30$ pF	0	—	16	ns
Output hold time, SD_CLK to CMD, DAT[0:7] change	t_{OH}	$C_L \leq 30$ pF	3	—	—	ns

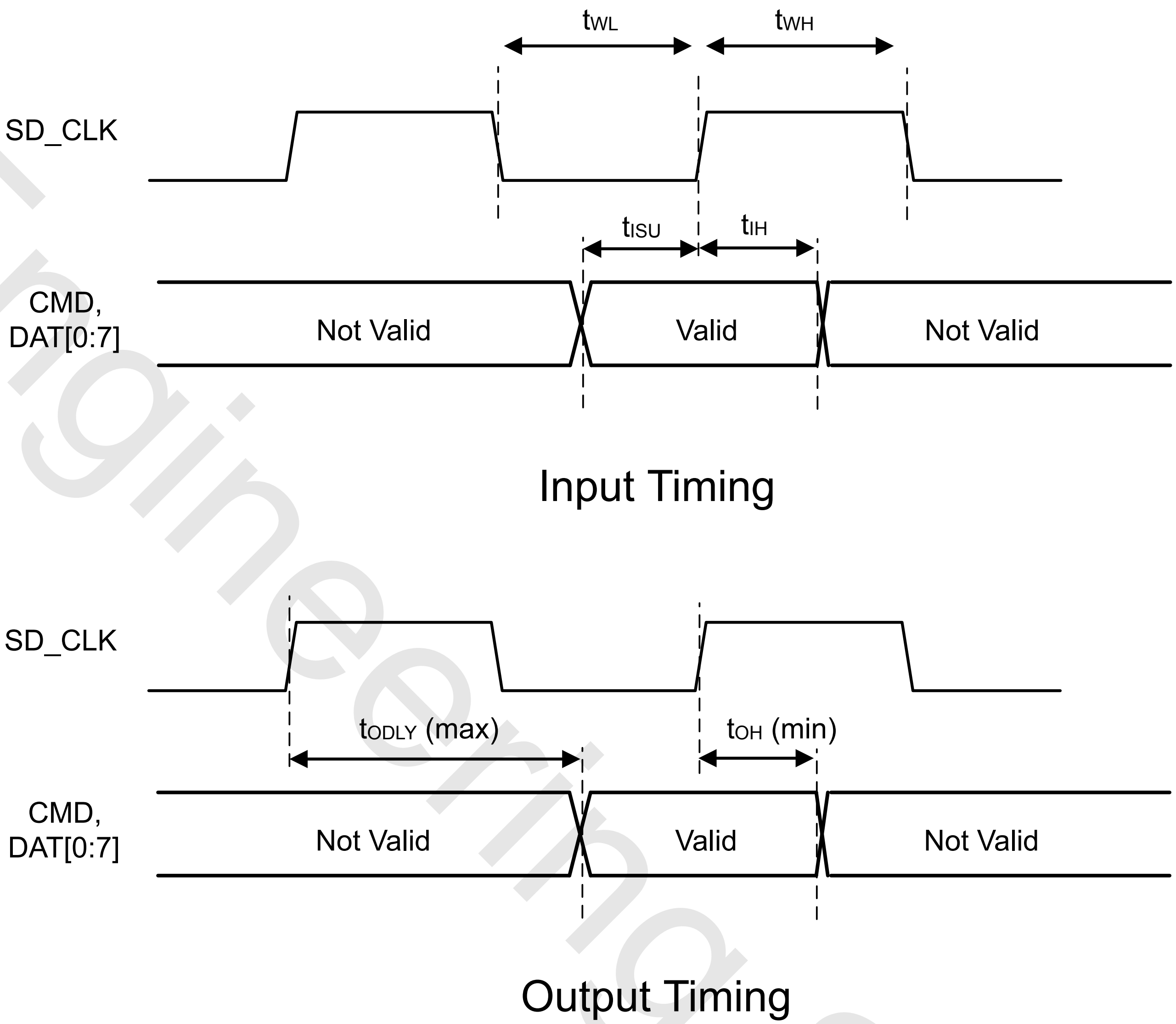


Figure 4.18. SDIO MMC SDR Mode Timing

SDIO MMC SDR Mode Timing at 3.0 V

Timing is specified for route location 0 at 3.0 V IOVDD with voltage scaling disabled and slew rate for SD_CLK set to 7, all other GPIO set to 6.

Table 4.51. SDIO MMC SDR Mode 3V Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	$C_L \leq 30$ pF	0	—	50	MHz
Clock low time	t_{WL}	$C_L \leq 30$ pF	9	—	10	ns
Clock high time	t_{WH}	$C_L \leq 30$ pF	9	—	10	ns
Clock rise time	t_R	$C_L \leq 30$ pF	1.96	3.87	—	ns
Clock fall time	t_F	$C_L \leq 30$ pF	1.67	3.31	—	ns
Input setup time, CMD, DAT[0:7] valid to SD_CLK	t_{ISU}	$C_L \leq 30$ pF	5.3	—	—	ns
Input hold time, SD_CLK to CMD, DAT[0:3] change	t_{IH}	$C_L \leq 30$ pF	2.5	—	—	ns
Output delay time, SD_CLK to CMD, DAT[0:7] valid	t_{ODLY}	$C_L \leq 30$ pF	0	—	16	ns
Output hold time, SD_CLK to CMD, DAT[0:7] change	t_{OH}	$C_L \leq 30$ pF	3	—	—	ns

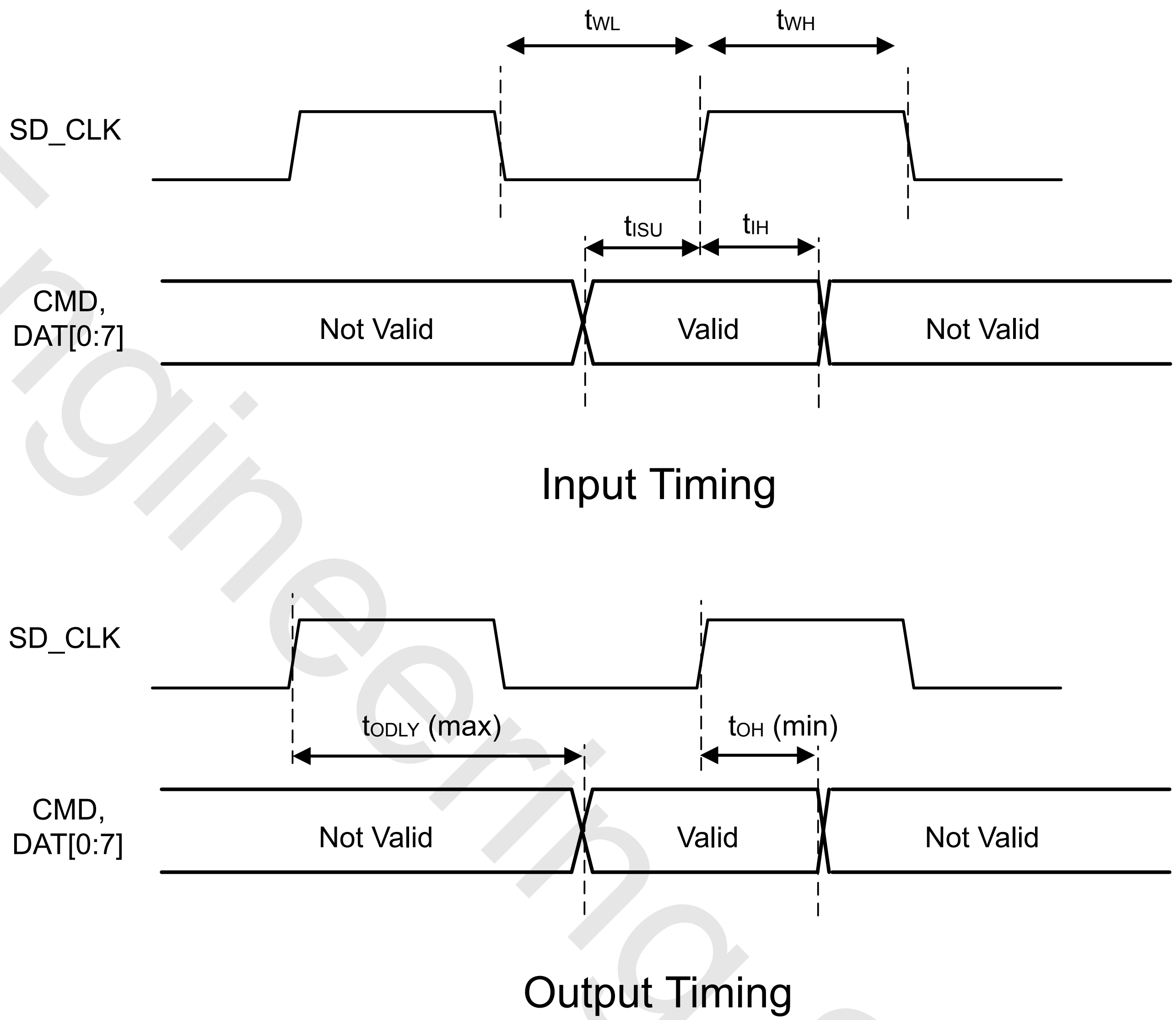


Figure 4.19. SDIO MMC SDR Mode Timing

SDIO MMC DDR Mode Timing

Timing is specified for route location 0 at 3.0 V or 1.8 V IOVDD with voltage scaling disabled and slew rate for SD_CLK set to 7, all other GPIO set to 6.

Table 4.52. SDR MMC DDR Mode Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Clock frequency during data transfer	F_{SD_CLK}	$C_L \leq 20$ pF	0	—	25	MHz
Clock low time	t_{WL}	$C_L \leq 20$ pF	18	—	20	ns
Clock high time	t_{WH}	$C_L \leq 20$ pF	18	—	20	ns
Clock rise time	t_R	$C_L \leq 20$ pF, 3.0 V IOVDD	1.13	2.37	—	ns
		$C_L \leq 20$ pF, 1.8 V IOVDD	1.13	5.21	—	ns
Clock fall time	t_F	$C_L \leq 20$ pF, 3.0 V IOVDD	1.01	2.02	—	ns
		$C_L \leq 20$ pF, 1.8 V IOVDD	1.01	4.10	—	ns
Input setup time, CMD valid to SD_CLK	t_{ISU}	$C_L \leq 20$ pF	5.3	—	—	ns
Input hold time, SD_CLK to CMD change	t_{IH}	$C_L \leq 20$ pF	2.5	—	—	ns
Output delay time, SD_CLK to CMD valid	t_{ODLY}	$C_L \leq 20$ pF	0	—	16	ns
Output hold time, SD_CLK to CMD change	t_{OH}	$C_L \leq 20$ pF	3	—	—	ns
Input setup time, DAT[0:7] valid to SD_CLK	t_{ISU2X}	$C_L \leq 20$ pF	5.3	—	—	ns
Input hold time, SD_CLK to DAT[0:7] change	t_{IH2X}	$C_L \leq 20$ pF	2.5	—	—	ns
Output delay time, SD_CLK to DAT[0:7] valid	t_{ODLY2X}	$C_L \leq 20$ pF	0	—	16	ns
Output hold time, SD_CLK to DAT[0:7] change	t_{OH2X}	$C_L \leq 20$ pF	3	—	—	ns

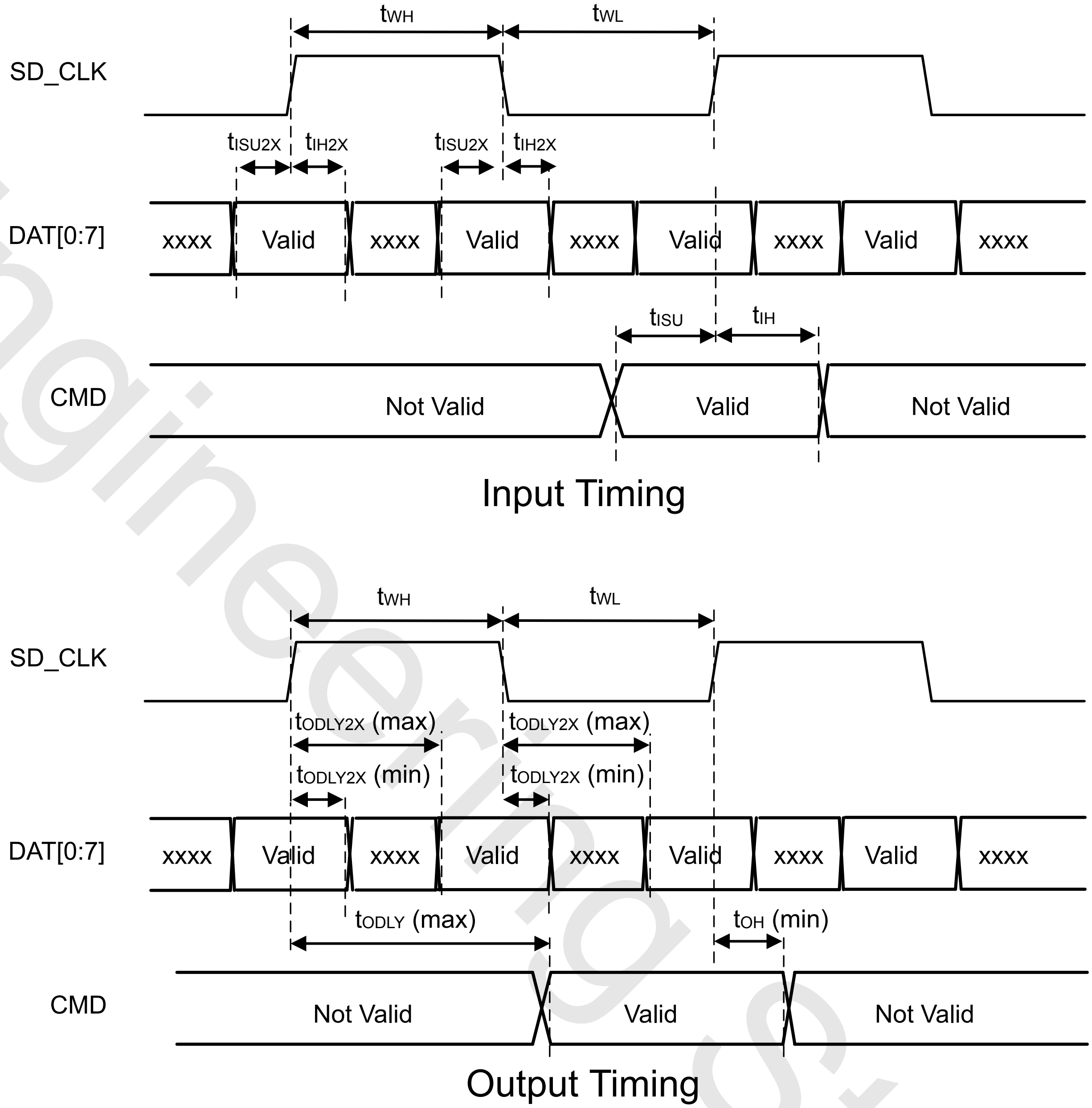


Figure 4.20. SDIO MMC DDR Mode Timing

4.1.27 Quad SPI (QSPI)

QSPI SDR Timing

Timing is specified at 3.0 V minimum IOVDD with voltage scaling disabled, route location 0 only, TX DLL = 23, RX DLL = 50, 25 pF loading per GPIO, and slew rate for all GPIO set to 6.

Table 4.53. QSPI SDR Mode Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK frequency	F_{SCLK}		—	—	30	MHz
Output valid	t_{OV}		—	—	12.2	ns
Output hold	t_{OH}		-1.6	—	—	ns
Input setup	t_{SU}		10.9	—	—	ns
Input hold	t_H		9.6	—	—	ns

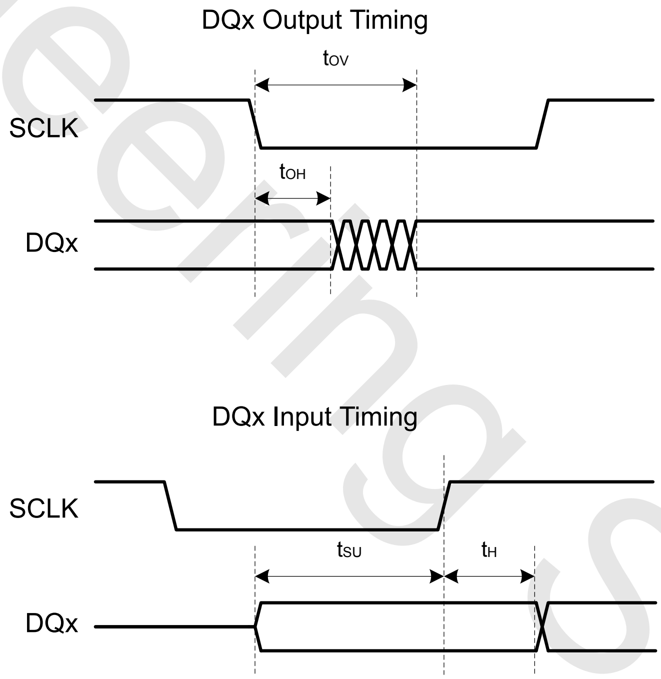


Figure 4.21. QSPI SDR Timing Diagrams

QSPI DDR Timing

Timing is specified at 3.0 V minimum IOVDD with voltage scaling disabled, route location 0 only, TX DLL = 43, RX DLL = 87, 25 pF loading per GPIO, and slew rate for all GPIO set to 6.

Table 4.54. QSPI DDR Mode Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK frequency	F_{SCLK}		—	—	15	MHz
Output valid	t_{OV}		—	—	24.5	ns
Output hold	t_{OH}		2.0	—	—	ns
Input setup	t_{SU}		20.8	—	—	ns
Input hold	t_{H}		-1.5	—	—	ns

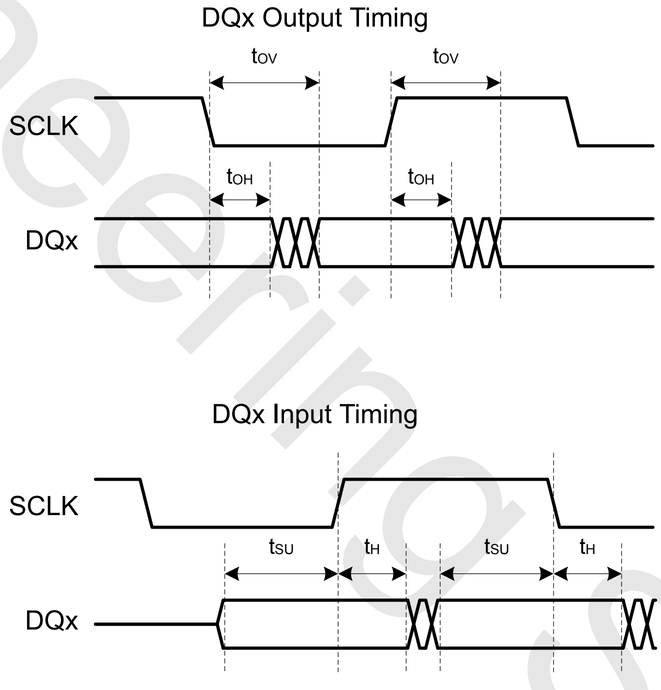


Figure 4.22. QSPI DDR Timing Diagrams

5. Pin Definitions

5.1 EFM32GG11B8xx in BGA192 Device Pinout

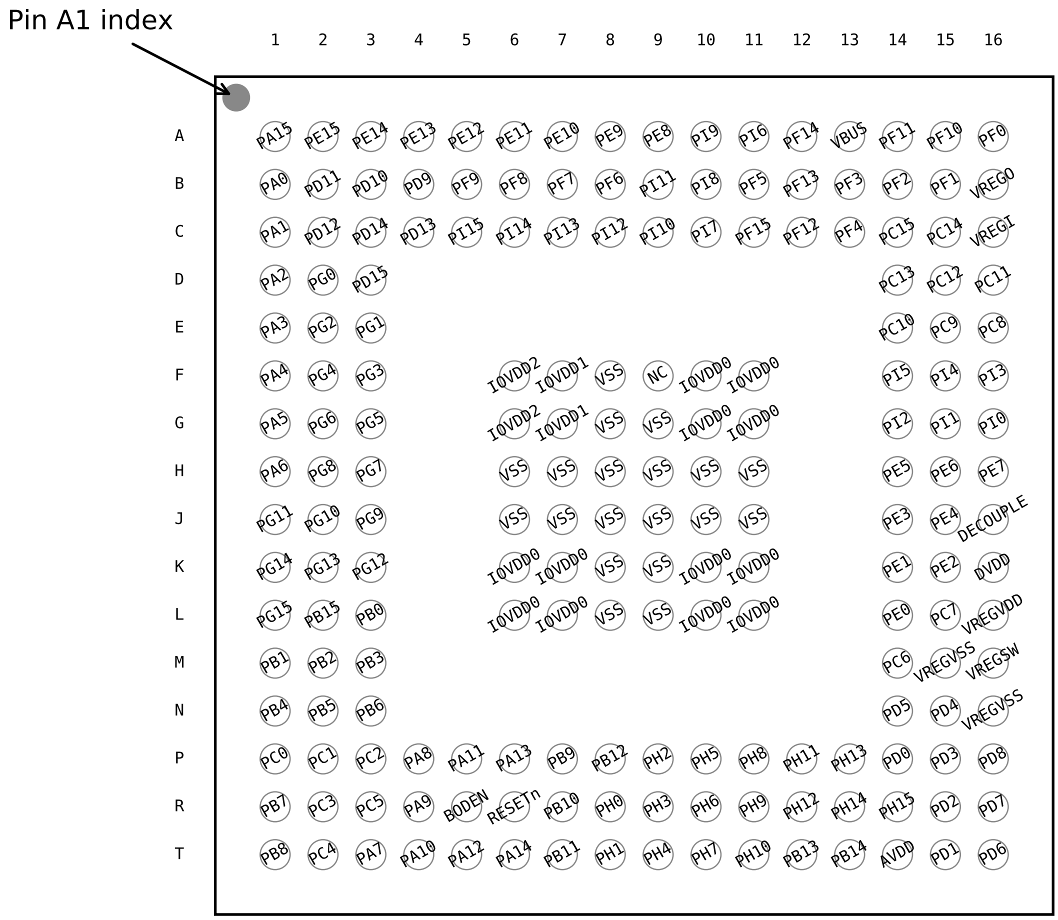


Figure 5.1. EFM32GG11B8xx in BGA192 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.3 GPIO Functionality Table or 5.4 Alternate Functionality Overview.

Table 5.1. EFM32GG11B8xx in BGA192 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA15	A1	GPIO	PE15	A2	GPIO
PE14	A3	GPIO	PE13	A4	GPIO
PE12	A5	GPIO	PE11	A6	GPIO
PE10	A7	GPIO	PE9	A8	GPIO
PE8	A9	GPIO	PI9	A10	GPIO (5V)
PI6	A11	GPIO (5V)	PF14	A12	GPIO (5V)

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
VBUS	A13	USB VBUS signal and auxiliary input to 5 V regulator.	PF11	A14	GPIO (5V)
PF10	A15	GPIO (5V)	PF0	A16	GPIO (5V)
PA0	B1	GPIO	PD11	B2	GPIO
PD10	B3	GPIO	PD9	B4	GPIO
PF9	B5	GPIO	PF8	B6	GPIO
PF7	B7	GPIO	PF6	B8	GPIO
PI11	B9	GPIO (5V)	PI8	B10	GPIO (5V)
PF5	B11	GPIO	PF13	B12	GPIO (5V)
PF3	B13	GPIO	PF2	B14	GPIO
PF1	B15	GPIO (5V)	VREGO	B16	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs
PA1	C1	GPIO	PD12	C2	GPIO
PD14	C3	GPIO (5V)	PD13	C4	GPIO (5V)
PI15	C5	GPIO (5V)	PI14	C6	GPIO (5V)
PI13	C7	GPIO (5V)	PI12	C8	GPIO (5V)
PI10	C9	GPIO (5V)	PI7	C10	GPIO (5V)
PF15	C11	GPIO (5V)	PF12	C12	GPIO
PF4	C13	GPIO	PC15	C14	GPIO (5V)
PC14	C15	GPIO (5V)	VREGI	C16	Input to 5 V regulator.
PA2	D1	GPIO	PG0	D2	GPIO (5V)
PD15	D3	GPIO (5V)	PC13	D14	GPIO (5V)
PC12	D15	GPIO (5V)	PC11	D16	GPIO (5V)
PA3	E1	GPIO	PG2	E2	GPIO (5V)
PG1	E3	GPIO (5V)	PC10	E14	GPIO (5V)
PC9	E15	GPIO (5V)	PC8	E16	GPIO (5V)
PA4	F1	GPIO	PG4	F2	GPIO (5V)
PG3	F3	GPIO (5V)	IOVDD2	F6 G6	Digital IO power supply 2.

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
IOVDD1	F7 G7	Digital IO power supply 1.	VSS	F8 G8 G9 H6 H7 H8 H9 H10 H11 J6 J7 J8 J9 J10 J11 K8 K9 L8 L9	Ground
NC	F9	No Connect.	IOVDD0	F10 F11 G10 G11 K6 K7 K10 K11 L6 L7 L10 L11	Digital IO power supply 0.
PI5	F14	GPIO (5V)	PI4	F15	GPIO (5V)
PI3	F16	GPIO (5V)	PA5	G1	GPIO
PG6	G2	GPIO (5V)	PG5	G3	GPIO (5V)
PI2	G14	GPIO (5V)	PI1	G15	GPIO (5V)
PI0	G16	GPIO (5V)	PA6	H1	GPIO
PG8	H2	GPIO (5V)	PG7	H3	GPIO (5V)
PE5	H14	GPIO	PE6	H15	GPIO
PE7	H16	GPIO	PG11	J1	GPIO (5V)
PG10	J2	GPIO (5V)	PG9	J3	GPIO (5V)
PE3	J14	GPIO	PE4	J15	GPIO
DECOUPLE	J16	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PG14	K1	GPIO
PG13	K2	GPIO	PG12	K3	GPIO
PE1	K14	GPIO (5V)	PE2	K15	GPIO
DVDD	K16	Digital power supply.	PG15	L1	GPIO (5V)
PB15	L2	GPIO (5V)	PB0	L3	GPIO
PE0	L14	GPIO (5V)	PC7	L15	GPIO
VREGVDD	L16	Voltage regulator VDD input	PB1	M1	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB2	M2	GPIO	PB3	M3	GPIO
PC6	M14	GPIO	VREGVSS	M15 N16	Voltage regulator VSS
VREGSW	M16	DCDC regulator switching node	PB4	N1	GPIO
PB5	N2	GPIO	PB6	N3	GPIO
PD5	N14	GPIO	PD4	N15	GPIO
PC0	P1	GPIO (5V)	PC1	P2	GPIO (5V)
PC2	P3	GPIO (5V)	PA8	P4	GPIO
PA11	P5	GPIO	PA13	P6	GPIO (5V)
PB9	P7	GPIO (5V)	PB12	P8	GPIO
PH2	P9	GPIO (5V)	PH5	P10	GPIO
PH8	P11	GPIO (5V)	PH11	P12	GPIO (5V)
PH13	P13	GPIO (5V)	PD0	P14	GPIO (5V)
PD3	P15	GPIO	PD8	P16	GPIO
PB7	R1	GPIO	PC3	R2	GPIO (5V)
PC5	R3	GPIO	PA9	R4	GPIO
BODEN	R5	Brown-Out Detector Enable. This pin may be left disconnected or tied to AVDD.	RESETn	R6	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.
PB10	R7	GPIO (5V)	PH0	R8	GPIO (5V)
PH3	R9	GPIO (5V)	PH6	R10	GPIO
PH9	R11	GPIO (5V)	PH12	R12	GPIO (5V)
PH14	R13	GPIO (5V)	PH15	R14	GPIO (5V)
PD2	R15	GPIO (5V)	PD7	R16	GPIO
PB8	T1	GPIO	PC4	T2	GPIO
PA7	T3	GPIO	PA10	T4	GPIO
PA12	T5	GPIO (5V)	PA14	T6	GPIO
PB11	T7	GPIO	PH1	T8	GPIO (5V)
PH4	T9	GPIO	PH7	T10	GPIO (5V)
PH10	T11	GPIO (5V)	PB13	T12	GPIO
PB14	T13	GPIO	AVDD	T14	Analog power supply.
PD1	T15	GPIO	PD6	T16	GPIO

Note:

1. GPIO with 5V tolerance are indicated by (5V).
2. The pins PD13, PD14, and PD15 will not be 5V tolerant on all future devices. In order to preserve upgrade options with full hardware compatibility, do not use these pins with 5V domains.

5.2 EFM32GG11B8xx in QFP100 Device Pinout

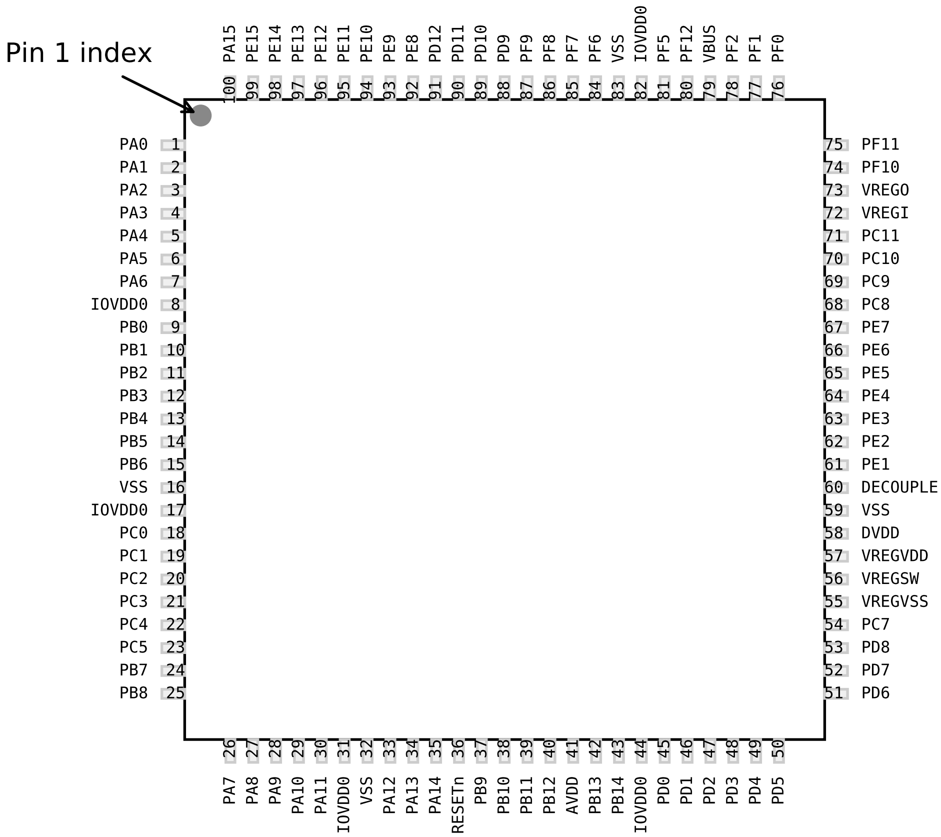


Figure 5.2. EFM32GG11B8xx in QFP100 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 5.3 GPIO Functionality Table or 5.4 Alternate Functionality Overview.

Table 5.2. EFM32GG11B8xx in QFP100 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PA0	1	GPIO	PA1	2	GPIO
PA2	3	GPIO	PA3	4	GPIO
PA4	5	GPIO	PA5	6	GPIO
PA6	7	GPIO	IOVDD0	8 17 31 44 82	Digital IO power supply 0.
PB0	9	GPIO	PB1	10	GPIO

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PB2	11	GPIO	PB3	12	GPIO
PB4	13	GPIO	PB5	14	GPIO
PB6	15	GPIO	VSS	16 32 59 83	Ground
PC0	18	GPIO (5V)	PC1	19	GPIO (5V)
PC2	20	GPIO (5V)	PC3	21	GPIO (5V)
PC4	22	GPIO	PC5	23	GPIO
PB7	24	GPIO	PB8	25	GPIO
PA7	26	GPIO	PA8	27	GPIO
PA9	28	GPIO	PA10	29	GPIO
PA11	30	GPIO	PA12	33	GPIO (5V)
PA13	34	GPIO (5V)	PA14	35	GPIO
RESETn	36	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.	PB9	37	GPIO (5V)
PB10	38	GPIO (5V)	PB11	39	GPIO
PB12	40	GPIO	AVDD	41	Analog power supply.
PB13	42	GPIO	PB14	43	GPIO
PD0	45	GPIO (5V)	PD1	46	GPIO
PD2	47	GPIO (5V)	PD3	48	GPIO
PD4	49	GPIO	PD5	50	GPIO
PD6	51	GPIO	PD7	52	GPIO
PD8	53	GPIO	PC7	54	GPIO
VREGVSS	55	Voltage regulator VSS	VREGSW	56	DCDC regulator switching node
VREGVDD	57	Voltage regulator VDD input	DVDD	58	Digital power supply.
DECOUPLE	60	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.	PE1	61	GPIO (5V)
PE2	62	GPIO	PE3	63	GPIO
PE4	64	GPIO	PE5	65	GPIO
PE6	66	GPIO	PE7	67	GPIO
PC8	68	GPIO (5V)	PC9	69	GPIO (5V)
PC10	70	GPIO (5V)	PC11	71	GPIO (5V)
VREGI	72	Input to 5 V regulator.	VREGO	73	Decoupling for 5 V regulator and regulator output. Power for USB PHY in USB-enabled OPNs
PF10	74	GPIO (5V)	PF11	75	GPIO (5V)
PF0	76	GPIO (5V)	PF1	77	GPIO (5V)

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PF2	78	GPIO	VBUS	79	USB VBUS signal and auxiliary input to 5 V regulator.
PF12	80	GPIO	PF5	81	GPIO
PF6	84	GPIO	PF7	85	GPIO
PF8	86	GPIO	PF9	87	GPIO
PD9	88	GPIO	PD10	89	GPIO
PD11	90	GPIO	PD12	91	GPIO
PE8	92	GPIO	PE9	93	GPIO
PE10	94	GPIO	PE11	95	GPIO
PE12	96	GPIO	PE13	97	GPIO
PE14	98	GPIO	PE15	99	GPIO
PA15	100	GPIO			

Note:

1. GPIO with 5V tolerance are indicated by (5V).

5.3 GPIO Functionality Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of each GPIO pin, followed by the functionality available on that pin. Refer to 5.4 Alternate Functionality Overview for a list of GPIO locations available for each function.

Table 5.3. GPIO Functionality Table

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PA15	BUSAY BUSBX LCD_SEG12	EBI_AD08 #0	TIM3_CC2 #0	ETH_MIIRXCLK #0 ETH_MDIO #3 US2_CLK #3	PRS_CH15 #0
PE15	BUSCY BUSDX LCD_SEG11	EBI_AD07 #0	TIM2_CDTI2 #2 TIM3_CC1 #0	ETH_RMIITXD0 #0 ETH_MIIRXD3 #0 SDIO_CMD #1 US0_RTS #0 QSPI0_DQS #1 LEU0_RX #2	PRS_CH14 #2 ETM_TD3 #4
PE14	BUSDY BUSCX LCD_SEG10	EBI_AD06 #0	TIM2_CDTI1 #2 TIM3_CC0 #0	ETH_RMIITXD1 #0 ETH_MIIRXD2 #0 SDIO_CLK #1 US0_CTS #0 QSPI0_SCLK #1 LEU0_TX #2	PRS_CH13 #2 ETM_TD2 #4
PE13	BUSCY BUSDX LCD_SEG9	EBI_AD05 #0	TIM1_CC3 #1 TIM2_CC2 #3 LE-TIM0_OUT1 #4	SDIO_CLK #0 ETH_MIIRXD1 #0 US0_TX #3 US0_CS #0 U1_RX #4 I2C0_SCL #6	LES_ALTEX7 PRS_CH2 #3 ACMP0_O #0 ETM_TD1 #4 GPIO_EM4WU5
PE12	BUSDY BUSCX LCD_SEG8	EBI_AD04 #0	TIM1_CC2 #1 TIM2_CC1 #3 WTIM0_CDTI2 #0 LETIM0_OUT0 #4	SDIO_CMD #0 ETH_MIIRXD0 #0 US0_RX #3 US0_CLK #0 U1_TX #4 I2C0_SDA #6	CMU_CLK1 #2 CMU_CLKI0 #6 LES_ALTEX6 PRS_CH1 #3 ETM_TD0 #4
PE11	BUSCY BUSDX LCD_SEG7	EBI_AD03 #0 EBI_CS3 #4	TIM1_CC1 #1 TIM4_CC2 #7 WTIM0_CDTI1 #0	SDIO_DAT0 #0 QSPI0_DQ7 #0 ETH_MIIRXDV #0 US0_RX #0	LES_ALTEX5 PRS_CH3 #2 ETM_TCLK #4
PE10	BUSDY BUSCX LCD_SEG6	EBI_AD02 #0 EBI_CS2 #4	TIM1_CC0 #1 TIM4_CC1 #7 WTIM0_CDTI0 #0	SDIO_DAT1 #0 QSPI0_DQ6 #0 ETH_MIIRXER #0 US0_TX #0	PRS_CH2 #2 GPIO_EM4WU9
PE9	BUSCY BUSDX LCD_SEG5	EBI_AD01 #0 EBI_CS1 #4	TIM4_CC0 #7 PCNT2_S1IN #1	SDIO_DAT2 #0 QSPI0_DQ5 #0 US5_RX #0	PRS_CH8 #2
PE8	BUSDY BUSCX LCD_SEG4	EBI_AD00 #0 EBI_CS0 #4	TIM2_CDTI0 #2 TIM4_CC2 #6 PCNT2_S0IN #1	SDIO_DAT3 #0 QSPI0_DQ4 #0 US5_TX #0 I2C2_SDA #0	PRS_CH3 #1
PI9		EBI_A14 #2	TIM1_CC3 #7 TIM4_CC1 #3	US4_CS #3	
PI6		EBI_A11 #2	TIM1_CC0 #7 TIM4_CC1 #2 WTIM3_CC0 #5	US4_TX #3	

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PF14	BUSDY BUSCX		TIM1_CC1 #6 TIM4_CC1 #1 TIM5_CC2 #7 WTIM3_CC1 #7	I2C2_SCL #4	
PF11	BUSCY BUSDX	EBI_NANDWEn #5	TIM5_CC2 #6 WTIM3_CC2 #3 PCNT2_S1IN #3	US5_CTS #2 U1_RX #1 I2C2_SCL #2 USB_DP	
PF10	BUSDY BUSCX	EBI_ARDY #5	TIM5_CC1 #6 WTIM3_CC1 #3 PCNT2_S0IN #3	US5_RTS #2 U1_TX #1 I2C2_SDA #2 USB_DM	
PF0	BUSDY BUSCX	EBI_A24 #1	TIM0_CC0 #4 WTIM0_CC1 #4 LE-TIM0_OUT0 #2	US2_TX #5 CAN0_RX #1 US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	PRS_CH15 #2 ACMP3_O #0 DBG_SWCLKTCK BOOT_TX
PA0	BUSBY BUSAX LCD_SEG13	EBI_AD09 #0 EBI_CSTFT #3	TIM0_CC0 #0 TIM0_CC1 #7 TIM3_CC0 #4 PCNT0_S0IN #4	ETH_RMIITXEN #0 ETH_MIITXCLK #0 SDIO_DAT0 #1 US1_RX #5 US3_TX #0 QSPI0_CS0 #1 LEU0_RX #4 I2C0_SDA #0	CMU_CLK2 #0 PRS_CH0 #0 PRS_CH3 #3 GPIO_EM4WU0
PD11	LCD_SEG30	EBI_CS2 #0 EBI_HSNC #1	TIM4_CC0 #6 WTIM3_CC2 #0	ETH_RMIICRSDV #1 SDIO_DAT5 #0 QSPI0_DQ2 #0 ETH_MIIRXD3 #2 US4_CLK #1	
PD10	LCD_SEG29	EBI_CS1 #0 EBI_VSNC #1	TIM4_CC2 #5 WTIM3_CC1 #0	ETH_RMIIREFCLK #1 SDIO_DAT6 #0 QSPI0_DQ1 #0 ETH_MIIRXD2 #2 US4_RX #1	CMU_CLK2 #5 CMU_CLKI0 #5
PD9	LCD_SEG28	EBI_CS0 #0 EBI_DTEN #1	TIM4_CC1 #5 WTIM3_CC0 #0	ETH_RMIIRXD0 #1 SDIO_DAT7 #0 QSPI0_DQ0 #0 ETH_MIIRXD1 #2 US4_TX #1	
PF9	BUSCY BUSDX LCD_SEG27	EBI_REn #4 EBI_BL1 #1	TIM4_CC0 #5	ETH_RMIIRXD1 #1 US2_CS #4 QSPI0_DQS #0 ETH_MIIRXD0 #2 ETH_TSUTMRTOG #3 SDIO_WP #0 U0_RTS #0 U1_CTS #1	ETM_TD0 #1
PF8	BUSDY BUSCX LCD_SEG26	EBI_WEn #4 EBI_BL0 #1	TIM0_CC2 #1 TIM4_CC2 #4	ETH_RMIITXEN #1 US2_CLK #4 QSPI0_CS1 #0 ETH_MIIRXDV #2 ETH_TSUEXTCLK #3 SDIO_CD #0 U0_CTS #0 U1_RTS #1	ETM_TCLK #1 GPIO_EM4WU8

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PF7	BUSCY BUSDX LCD_SEG25	EBI_BL1 #0 EBI_BL1 #4 EBI_BL1 #5 EBI_DCLK #1	TIM0_CC1 #1 TIM4_CC1 #4	ETH_RMIITXD0 #1 US2_RX #4 QSPI0_CS0 #0 ETH_MIIRXER #2 US1_RX #3 U0_RX #0	PRS_CH23 #2
PF6	BUSDY BUSCX LCD_SEG24	EBI_BL0 #0 EBI_BL0 #4 EBI_BL0 #5 EBI_CSTFT #1	TIM0_CC0 #1 TIM4_CC0 #4 WTIM3_CC2 #5	ETH_RMIITXD1 #1 US2_TX #4 QSPI0_SCLK #0 US1_TX #3 U0_TX #0	PRS_CH22 #2
PI11				US4_RTS #3	
PI8		EBI_A13 #2	TIM1_CC2 #7 TIM4_CC0 #3	US4_CLK #3	
PF5	BUSCY BUSDX LCD_SEG3	EBI_REn #0 EBI_REn #5 EBI_A27 #1	TIM0_CDTI2 #2 TIM1_CC3 #6 TIM4_CC0 #2	US2_CS #5 I2C2_SCL #0 USB_VBUSEN	PRS_CH2 #1 DBG_TDI
PF13	BUSCY BUSDX		TIM1_CC0 #6 TIM4_CC0 #1 TIM5_CC1 #7 WTIM3_CC0 #7	US5_CLK #2 I2C2_SDA #4	
PF3	BUSCY BUSDX LCD_SEG1	EBI_ALE #0	TIM4_CC0 #0 TIM0_CDTI0 #2 TIM1_CC1 #5	CAN1_TX #1 US1_CTS #2 I2C2_SCL #5	CMU_CLK1 #4 PRS_CH0 #1 ETM_TD3 #1
PF2	BUSDY BUSCX LCD_SEG0	EBI_ARDY #0 EBI_A26 #1	TIM0_CC2 #4 TIM1_CC0 #5 TIM2_CC0 #3	US2_CLK #5 CAN0_TX #1 US1_TX #5 U0_RX #5 LEU0_TX #4 I2C1_SCL #4	CMU_CLK0 #4 PRS_CH0 #3 ACMP1_O #0 DBG_TDO DBG_SWO #0 GPIO_EM4WU4
PF1	BUSCY BUSDX	EBI_A25 #1	TIM0_CC1 #4 WTIM0_CC2 #4 LE-TIM0_OUT1 #2	US2_RX #5 CAN1_RX #1 US1_CS #2 U0_TX #5 LEU0_RX #3 I2C0_SCL #5	PRS_CH4 #2 DBG_SWDIOTMS GPIO_EM4WU3 BOOT_RX
PA1	BUSAY BUSBX LCD_SEG14	EBI_AD10 #0 EBI_DCLK #3	TIM0_CC0 #7 TIM0_CC1 #0 TIM3_CC1 #4 PCNT0_S1IN #4	ETH_RMIIRXD1 #0 ETH_MIITXD3 #0 SDIO_DAT1 #1 US3_RX #0 QSPI0_CS1 #1 I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0
PD12	LCD_SEG31	EBI_CS3 #0	TIM4_CC1 #6	ETH_RMIIRXER #1 SDIO_DAT4 #0 QSPI0_DQ3 #0 ETH_MIIRXCLK #2 US4_CS #1	
PD14		EBI_NANDWEn #1	TIM2_CDTI1 #1 TIM3_CC2 #6 WTIM0_CC2 #1	ETH_MDC #1 CAN0_RX #5 US4_RTS #1 US5_CS #1 I2C0_SDA #3	

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PD13		EBI_ARDY #1	TIM2_CDTI0 #1 TIM3_CC1 #6 WTIM0_CC1 #1	ETH_MDIO #1 US4_CTS #1 US5_CLK #1	ETM_TD1 #1
PI15				CAN1_TX #7 US3_CS #5	
PI14				CAN1_RX #7 US3_CLK #5	
PI13				CAN0_TX #7 US3_RX #5	
PI12				CAN0_RX #7 US3_TX #5	
PI10		EBI_A15 #2	TIM4_CC2 #3	US4_CTS #3	
PI7		EBI_A12 #2	TIM1_CC1 #7 TIM4_CC2 #2 WTIM3_CC1 #5	US4_RX #3	
PF15	BUSCY BUSDX		TIM1_CC2 #6 TIM4_CC2 #1 WTIM3_CC2 #7	US5_TX #2 I2C2_SDA #5	
PF12	BUSDY BUSCX	EBI_NANDREn #5	TIM4_CC2 #0 TIM1_CC3 #5 TIM5_CC0 #7 WTIM3_CC2 #6	US5_CS #2 I2C2_SCL #3 USB_ID	
PF4	BUSDY BUSCX LCD_SEG2	EBI_WEn #0 EBI_WEn #5	TIM4_CC1 #0 TIM0_CDTI1 #2 TIM1_CC2 #5 WTIM3_CC1 #6	US1_RTS #2 I2C2_SDA #3	PRS_CH1 #1
PC15	VDAC0_OUT1ALT / OPA1_OUTALT #3 BUSACMP1Y BU-SACMP1X	EBI_NANDREn #4	TIM0_CDTI2 #1 TIM1_CC2 #0 WTIM0_CC0 #4 LE-TIM0_OUT1 #5	US0_CLK #3 US1_CLK #3 US3_RTS #3 U0_RX #3 U1_RTS #0 LEU0_RX #5 I2C2_SCL #1	LES_CH15 PRS_CH1 #2 ACMP3_O #1 DBG_SWO #1
PC14	VDAC0_OUT1ALT / OPA1_OUTALT #2 BUSACMP1Y BU-SACMP1X	EBI_NANDWEn #4	TIM0_CDTI1 #1 TIM1_CC1 #0 TIM1_CC3 #4 TIM5_CC0 #6 WTIM3_CC0 #3 LE-TIM0_OUT0 #5 PCNT0_S1IN #0	US0_CS #3 US1_CS #3 US2_RTS #3 US3_CS #2 U0_TX #3 U1_CTS #0 LEU0_TX #5 I2C2_SDA #1	LES_CH14 PRS_CH0 #2 ACMP3_O #2
PA2	BUSBY BUSAX LCD_SEG15	EBI_AD11 #0 EBI_DTEN #3	TIM0_CC2 #0 TIM3_CC2 #4	ETH_RMIIRXD0 #0 ETH_MIITXD2 #0 SDIO_DAT2 #1 US1_RX #6 US3_CLK #0 QSPI0_DQ0 #1	CMU_CLK0 #0 PRS_CH8 #1 ETM_TD0 #3
PG0	BUSACMP2Y BU-SACMP2X	EBI_AD00 #2	TIM6_CC0 #0 TIM2_CDTI0 #3 WTIM0_CDTI1 #1 LETIM1_OUT0 #6	ETH_MIITXCLK #1 US3_TX #4 QSPI0_SCLK #2	CMU_CLK2 #3

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PD15		EBI_NANDREn #1	TIM2_CDTI2 #1 TIM3_CC0 #7 WTIM0_CDTI0 #1 PCNT1_S0IN #2	ETH_TSUEXTCLK #1 CAN0_TX #5 US5_CTS #1 I2C0_SCL #3	
PC13	VDAC0_OUT1ALT / OPA1_OUTALT #1 BUSACMP1Y BU-SACMP1X	EBI_ARDY #4	TIM0_CDTI0 #1 TIM1_CC0 #0 TIM1_CC2 #4 TIM5_CC2 #5 WTIM3_CC2 #2 PCNT0_S0IN #0 PCNT2_S1IN #4	US0_CTS #3 US1_RTS #4 US2_RTS #4 U0_CTS #3 U1_RX #0 I2C2_SCL #6	LES_CH13 PRS_CH21 #1 ACMP3_O #3
PC12	VDAC0_OUT1ALT / OPA1_OUTALT #0 BUSACMP1Y BU-SACMP1X		TIM1_CC3 #0 TIM5_CC1 #5 WTIM3_CC1 #2 PCNT2_S0IN #4	CAN1_RX #4 US0_RTS #3 US1_CTS #4 US2_CTS #4 U0_RTS #3 U1_TX #0 I2C2_SDA #6	CMU_CLK0 #1 LES_CH12 PRS_CH20 #1
PC11	BUSACMP1Y BU-SACMP1X	EBI_ALE #4 EBI_ALE #5 EBI_A23 #1	TIM5_CC0 #5 WTIM3_CC0 #2	CAN1_TX #4 US0_TX #2 I2C1_SDA #4	LES_CH11 PRS_CH19 #1
PA3	BUSAY BUSBX LCD_SEG16	EBI_AD12 #0 EBI_VSNC #3	TIM0_CDTI0 #0 TIM3_CC0 #5	ETH_RMIIREFCLK #0 ETH_MIITXD1 #0 SDIO_DAT3 #1 US3_CS #0 U0_TX #2 QSPI0_DQ1 #1	CMU_CLK2 #1 CMU_CLKI0 #1 CMU_CLK2 #4 LES_ALTEX2 PRS_CH9 #1 ETM_TD1 #3
PG2	BUSACMP2Y BU-SACMP2X	EBI_AD02 #2	TIM6_CC2 #0 TIM2_CDTI2 #3 WTIM0_CC0 #2 LE-TIM1_OUT0 #7	ETH_MIITXD2 #1 US3_CLK #4 QSPI0_DQ1 #2	CMU_CLK0 #3
PG1	BUSACMP2Y BU-SACMP2X	EBI_AD01 #2	TIM6_CC1 #0 TIM2_CDTI1 #3 WTIM0_CDTI2 #1 LETIM1_OUT1 #6	ETH_MIITXD3 #1 US3_RX #4 QSPI0_DQ0 #2	CMU_CLK1 #3
PC10	BUSACMP1Y BU-SACMP1X	EBI_A10 #2 EBI_A22 #1	TIM2_CC2 #2 TIM5_CC2 #4 WTIM3_CC2 #1	CAN1_TX #3 US0_RX #2	LES_CH10 PRS_CH18 #1
PC9	BUSACMP1Y BU-SACMP1X	EBI_A09 #2 EBI_A21 #1 EBI_A27 #3	TIM2_CC1 #2 TIM5_CC1 #4 WTIM3_CC1 #1	CAN1_RX #3 US0_CLK #2	LES_CH9 PRS_CH5 #0 GPIO_EM4WU2
PC8	BUSACMP1Y BU-SACMP1X	EBI_A08 #2 EBI_A15 #0 EBI_A20 #1 EBI_A26 #3	TIM2_CC0 #2 TIM5_CC0 #4 WTIM3_CC0 #1	US0_CS #2	LES_CH8 PRS_CH4 #0
PA4	BUSBY BUSAX LCD_SEG17	EBI_AD13 #0 EBI_HSNC #3	TIM0_CDTI1 #0 TIM3_CC1 #5	ETH_RMIICRSDV #0 ETH_MIITXD0 #0 SDIO_DAT4 #1 US3_CTS #0 U0_RX #2 QSPI0_DQ2 #1	LES_ALTEX3 PRS_CH16 #0 ETM_TD2 #3
PG4	BUSACMP2Y BU-SACMP2X	EBI_AD04 #2	TIM6_CDTI1 #0 WTIM0_CC2 #2	ETH_MIITXD0 #1 US3_CTS #4 QSPI0_DQ3 #2	

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PG3	BUSACMP2Y BU-SACMP2X	EBI_AD03 #2	TIM6_CDTI0 #0 WTIM0_CC1 #2 LE-TIM1_OUT1 #7	ETH_MIITXD1 #1 US3_CS #4 QSPI0_DQ2 #2	
PI5		EBI_A07 #2	WTIM3_CC2 #4	US4_RTS #2 I2C2_SCL #7	ACMP3_O #5
PI4		EBI_A06 #2	WTIM3_CC1 #4	US4_CTS #2 I2C2_SDA #7	ACMP3_O #4
PI3		EBI_A05 #2	WTIM3_CC0 #4	US4_CS #2 I2C1_SCL #7	
PA5	BUSAY BUSBX LCD_SEG18	EBI_AD14 #0	TIM0_CDTI2 #0 TIM3_CC2 #5 PCNT1_S0IN #0	ETH_RMIIRXER #0 ETH_MIITXEN #0 SDIO_DAT5 #1 US3_RTS #0 U0_CTS #2 QSPI0_DQ3 #1 LEU1_TX #1	LES_ALTEX4 PRS_CH17 #0 ACMP1_O #7 ETM_TD3 #3
PG6	BUSACMP2Y BU-SACMP2X	EBI_AD06 #2	TIM2_CC1 #7 TIM6_CC0 #1	ETH_MIITXER #1 US3_TX #3 QSPI0_DQ5 #2	
PG5	BUSACMP2Y BU-SACMP2X	EBI_AD05 #2	TIM6_CDTI2 #0 TIM2_CC0 #7	ETH_MIITXEN #1 US3_RTS #4 QSPI0_DQ4 #2	
PI2		EBI_A04 #2	TIM5_CC2 #3 WTIM1_CC3 #5 PCNT2_S0IN #5	US4_CLK #2 I2C1_SDA #7	ACMP2_O #5
PI1		EBI_A03 #2	TIM5_CC1 #3 WTIM1_CC2 #5 PCNT2_S1IN #5	US4_RX #2	ACMP2_O #4
PI0		EBI_A02 #2	TIM5_CC0 #3 WTIM1_CC1 #5 PCNT2_S0IN #6	US4_TX #2	ACMP2_O #3
PA6	BUSBY BUSAX LCD_SEG19	EBI_AD15 #0	TIM3_CC0 #6 WTIM0_CC0 #1 LE-TIM1_OUT1 #0 PCNT1_S1IN #0	ETH_MIITXER #0 ETH_MDC #3 SDIO_CD #2 US5_TX #1 U0_RTS #2 LEU1_RX #1	PRS_CH6 #0 ACMP0_O #4 ETM_TCLK #3 GPIO_EM4WU1
PG8		EBI_AD08 #2	TIM2_CC0 #6 TIM6_CC2 #1 WTIM0_CC0 #3	ETH_MIIRXD3 #1 CAN0_RX #4 US3_CLK #3 QSPI0_DQ7 #2	
PG7	BUSACMP2Y BU-SACMP2X	EBI_AD07 #2	TIM2_CC2 #7 TIM6_CC1 #1	ETH_MIIRXCLK #1 US3_RX #3 QSPI0_DQ6 #2	
PE5	BUSCY BUSDX LCD_COM1	EBI_A12 #0 EBI_A17 #1 EBI_A23 #3	TIM3_CC0 #3 TIM3_CC2 #2 TIM5_CC1 #0 TIM6_CDTI1 #2 WTIM0_CC1 #0 WTIM1_CC2 #4	US0_CLK #1 US1_CLK #6 US3_CTS #1 U1_RTS #3 I2C0_SCL #7	PRS_CH17 #2

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PE6	BUSDY BUSCX LCD_COM2	EBI_A13 #0 EBI_A18 #1 EBI_A24 #3	TIM3_CC1 #3 TIM5_CC2 #0 TIM6_CDTI2 #2 WTIM0_CC2 #0 WTIM1_CC3 #4	US0_RX #1 US3_TX #1	PRS_CH6 #2
PE7	BUSCY BUSDX LCD_COM3	EBI_A14 #0 EBI_A19 #1 EBI_A25 #3	TIM3_CC2 #3 TIM5_CC0 #1 WTIM1_CC0 #5	US0_TX #1 US3_RX #1	PRS_CH7 #2
PG11		EBI_AD11 #2	TIM6_CDTI2 #1 WTIM0_CDTI0 #3	ETH_MIIRXD0 #1 CAN1_TX #6 US3_RTS #5 QSPI0_DQS #2	ETM_TD3 #5
PG10		EBI_AD10 #2	TIM2_CC2 #6 TIM6_CDTI1 #1 WTIM0_CC2 #3	ETH_MIIRXD1 #1 CAN1_RX #6 US3_CTS #3 QSPI0_CS1 #2	
PG9		EBI_AD09 #2	TIM2_CC1 #6 TIM6_CDTI0 #1 WTIM0_CC1 #3	ETH_MIIRXD2 #1 CAN0_TX #4 US3_CTS #5 QSPI0_CS0 #2	
PE3	BU_STAT	EBI_A10 #0 EBI_A15 #1	TIM3_CC0 #2 WTIM1_CC0 #4	US0_CTS #1 U0_RTS #1 U1_RX #3	ACMP1_O #1
PE4	BUSDY BUSCX LCD_COM0	EBI_A11 #0 EBI_A16 #1 EBI_A22 #3	TIM3_CC1 #2 TIM5_CC0 #0 TIM6_CDTI0 #2 WTIM0_CC0 #0 WTIM1_CC1 #4	US0_CS #1 US1_CS #5 US3_CS #1 U0_RX #6 U1_CTS #3 I2C0_SDA #7	PRS_CH16 #2
PG14		EBI_AD14 #2	TIM6_CC2 #2 WTIM2_CC0 #4 PCNT1_S0IN #7	ETH_MIICRS #1 US0_CLK #6	ETM_TD0 #5
PG13		EBI_AD13 #2	TIM6_CC1 #2 WTIM0_CDTI2 #3 WTIM2_CC2 #3	ETH_MIIRXER #1 US0_RX #6	ETM_TD1 #5
PG12		EBI_AD12 #2	TIM6_CC0 #2 WTIM0_CDTI1 #3 WTIM2_CC1 #3	ETH_MIIRXDV #1 US0_TX #6	ETM_TD2 #5
PE1	BUSCY BUSDX	EBI_A01 #2 EBI_A08 #0	TIM3_CC1 #1 WTIM1_CC2 #3 PCNT0_S1IN #1	CAN0_TX #6 U0_RX #1 I2C1_SCL #2	CMU_CLKI0 #4 PRS_CH23 #1 ACMP2_O #2
PE2	BU_VOUT	EBI_A09 #0 EBI_A14 #1	TIM3_CC2 #1 WTIM1_CC3 #3	US0_RTS #1 U0_CTS #1 U1_TX #3	PRS_CH20 #2 ACMP0_O #1
PG15		EBI_AD15 #2	WTIM2_CC1 #4 PCNT1_S1IN #7	ETH_MIICOL #1 US0_CS #6	ETM_TCLK #5
PB15	BUSAY BUSBX	EBI_CS3 #1 EBI_ARDY #2	TIM3_CC1 #7	ETH_TSUTMRTOG #1 SDIO_WP #2 US2_RTS #1 US5_RTS #1	PRS_CH17 #1 ETM_TD2 #1

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PB0	BUSBY BUSAX LCD_SEG32	EBI_AD00 #1 EBI_CS0 #3 EBI_A16 #0	TIM2_CDTI0 #0 TIM1_CC0 #2 TIM3_CC2 #7 WTIM0_CC0 #5 PCNT0_S0IN #5 PCNT1_S1IN #2	LEU1_TX #3	PRS_CH4 #1 ACMP0_O #5
PE0	BUSDY BUSCX	EBI_A00 #2 EBI_A07 #0	TIM3_CC0 #1 WTIM1_CC1 #3 PCNT0_S0IN #1	CAN0_RX #6 U0_TX #1 I2C1_SDA #2	PRS_CH22 #1 ACMP2_O #1
PC7	BUSACMP0Y BU-SACMP0X OPA3_N	EBI_A06 #0 EBI_A13 #1 EBI_A21 #3	WTIM1_CC0 #3	US0_CTS #2 US1_RTS #3 LEU1_RX #0 I2C0_SCL #2	LES_CH7 PRS_CH15 #1 ETM_TD0 #2
PB1	BUSAY BUSBX LCD_SEG33	EBI_AD01 #1 EBI_CS1 #3 EBI_A17 #0	TIM2_CDTI1 #0 TIM1_CC1 #2 WTIM0_CC1 #5 LE-TIM1_OUT1 #5 PCNT0_S1IN #5	ETH_MIICRS #0 US5_RX #2 LEU1_RX #3	PRS_CH5 #1
PB2	BUSBY BUSAX LCD_SEG34	EBI_AD02 #1 EBI_CS2 #3 EBI_A18 #0	TIM2_CDTI2 #0 TIM1_CC2 #2 WTIM0_CC2 #5 LE-TIM1_OUT0 #5	ETH_MIICOL #0 US1_CS #6	PRS_CH18 #0 ACMP0_O #6
PB3	BUSAY BUSBX LCD_SEG20 / LCD_COM4	EBI_AD03 #1 EBI_CS3 #3 EBI_A19 #0	TIM1_CC3 #2 WTIM0_CC0 #6 PCNT1_S0IN #1	ETH_MIICRS #2 ETH_MDIO #0 SDIO_DAT6 #1 US2_TX #1 US3_TX #2 QSPI0_DQ4 #1	PRS_CH19 #0 ACMP0_O #7
PC6	BUSACMP0Y BU-SACMP0X OPA3_P	EBI_A05 #0	WTIM1_CC3 #2	US0_RTS #2 US1_CTS #3 LEU1_TX #0 I2C0_SDA #2	LES_CH6 PRS_CH14 #1 ETM_TCLK #2
PB4	BUSBY BUSAX LCD_SEG21 / LCD_COM5	EBI_AD04 #1 EBI_ARDY #3 EBI_A20 #0	WTIM0_CC1 #6 PCNT1_S1IN #1	ETH_MIICOL #2 ETH_MDC #0 SDIO_DAT7 #1 US2_RX #1 QSPI0_DQ5 #1 LEU1_TX #4	PRS_CH20 #0
PB5	BUSAY BUSBX LCD_SEG22 / LCD_COM6	EBI_AD05 #1 EBI_ALE #3 EBI_A21 #0	WTIM0_CC2 #6 LE-TIM1_OUT0 #4 PCNT0_S0IN #6	ETH_TSUEXTCLK #0 US0_RTS #4 US2_CLK #1 QSPI0_DQ6 #1 LEU1_RX #4	PRS_CH21 #0
PB6	BUSBY BUSAX LCD_SEG23 / LCD_COM7	EBI_AD06 #1 EBI_WEn #3 EBI_A22 #0	TIM0_CC0 #3 TIM2_CC0 #4 WTIM3_CC0 #6 LE-TIM1_OUT1 #4 PCNT0_S1IN #6	ETH_TSUTMRTOG #0 US0_CTS #4 US2_CS #1 QSPI0_DQ7 #1	PRS_CH12 #1
PD5	BUSADC0Y BU-SADC0X OPA2_OUT	EBI_A09 #1 EBI_A18 #3	TIM6_CC1 #7 WTIM0_CDTI1 #4 WTIM1_CC3 #1 WTIM2_CC2 #5	US1_RTS #1 U0_CTS #5 LEU0_RX #0 I2C1_SCL #3	PRS_CH11 #2 ETM_TD3 #0 ETM_TD3 #2

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PD4	BUSADC0Y BUSADC0X OPA2_P	EBI_A08 #1 EBI_A17 #3	TIM6_CC0 #7 WTIM0_CDTI0 #4 WTIM1_CC2 #1 WTIM2_CC1 #5	CAN1_TX #2 US1_CTS #1 US3_CLK #2 LEU0_TX #0 I2C1_SDA #3	CMU_CLKI0 #0 PRS_CH10 #2 ETM_TD2 #0 ETM_TD2 #2
PC0	VDAC0_OUT0ALT / OPA0_OUTALT #0 BUSACMP0Y BUSACMP0X	EBI_AD07 #1 EBI_CS0 #2 EBI_REn #3 EBI_A23 #0	TIM0_CC1 #3 TIM2_CC1 #4 PCNT0_S0IN #2	ETH_MDIO #2 CAN0_RX #0 US0_TX #5 US1_TX #0 US1_CS #4 US2_RTS #0 US3_CS #3 I2C0_SDA #4	LES_CH0 PRS_CH2 #0
PC1	VDAC0_OUT0ALT / OPA0_OUTALT #1 BUSACMP0Y BUSACMP0X	EBI_AD08 #1 EBI_CS1 #2 EBI_BL0 #3 EBI_A24 #0	TIM0_CC2 #3 TIM2_CC2 #4 WTIM0_CC0 #7 PCNT0_S1IN #2	ETH_MDC #2 CAN0_TX #0 US0_RX #5 US1_TX #4 US1_RX #0 US2_CTS #0 US3_RTS #1 I2C0_SCL #4	LES_CH1 PRS_CH3 #0
PC2	VDAC0_OUT0ALT / OPA0_OUTALT #2 BUSACMP0Y BUSACMP0X	EBI_AD09 #1 EBI_CS2 #2 EBI_NANDWEn #3 EBI_A25 #0	TIM0_CDTI0 #3 TIM2_CC0 #5 WTIM0_CC1 #7 LETIM1_OUT0 #3	ETH_TSUEXTCLK #2 CAN1_RX #0 US1_RX #4 US2_TX #0	LES_CH2 PRS_CH10 #1
PA8	BUSBY BUSAX LCD_SEG36	EBI_AD14 #1 EBI_A02 #3 EBI_DCLK #0	TIM2_CC0 #0 TIM0_CC0 #6 LETIM0_OUT0 #6 PCNT1_S1IN #4	US2_RX #2 US4_RTS #0	PRS_CH8 #0
PA11	BUSAY BUSBX LCD_SEG39	EBI_CS1 #1 EBI_A05 #3 EBI_HSNC #0	WTIM2_CC2 #0 LETIM1_OUT0 #1	US2_CTS #2	PRS_CH11 #0
PA13	BUSAY BUSBX	EBI_WEn #1 EBI_NANDWEn #2 EBI_A01 #0 EBI_A07 #3	TIM0_CC2 #7 TIM2_CC1 #1 WTIM0_CDTI1 #2 WTIM2_CC1 #1 LETIM1_OUT1 #1 PCNT1_S1IN #5	CAN1_TX #5 US0_CS #5 US2_TX #3	PRS_CH13 #0
PB9	BUSAY BUSBX	EBI_ALE #1 EBI_NANDREn #2 EBI_A00 #1 EBI_A03 #0 EBI_A09 #3	WTIM2_CC0 #2 LETIM0_OUT0 #7	SDIO_WP #3 CAN0_RX #3 US1_CTS #0 U1_TX #2	PRS_CH13 #1 ACMP1_O #5
PB12	BUSBY BUSAX VDAC0_OUT1 / OPA1_OUT	EBI_A03 #1 EBI_A12 #3 EBI_CSTFT #2	TIM1_CC3 #3 WTIM2_CC0 #3 LETIM0_OUT1 #1 PCNT0_S0IN #7 PCNT1_S1IN #6	US2_CTS #1 US5_RTS #0 U1_RTS #2 I2C1_SCL #1	PRS_CH16 #1
PH2	BUSADC1Y BUSADC1X	EBI_VSNC #2	TIM6_CC0 #3	US1_CTS #6	
PH5	BUSADC1Y BUSADC1X	EBI_A17 #2	TIM6_CDTI0 #3 WTIM2_CC1 #6	US4_RX #4	
PH8	BUSACMP3Y BUSACMP3X	EBI_A20 #2	TIM6_CC0 #4 WTIM1_CC0 #6 WTIM2_CC1 #7	US4_CTS #4	

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PH11	BUSACMP3Y BU-SACMP3X	EBI_A23 #2	TIM5_CC1 #1 WTIM1_CC3 #6	US5_RX #3 U1_TX #5 I2C1_SDA #5	
PH13	BUSACMP3Y BU-SACMP3X	EBI_A25 #2	TIM5_CC0 #2 WTIM1_CC1 #7 PCNT2_S1IN #7	US5_CS #3 U1_CTS #5 I2C1_SDA #6	
PD0	VDAC0_OUT0ALT / OPA0_OUTALT #4 OPA2_OUTALT BU-SADC0Y BUSADC0X	EBI_A04 #1 EBI_A13 #3	TIM4_CDTI0 TIM6_CC2 #5 WTIM1_CC2 #0 PCNT2_S0IN #0	CAN0_RX #2 US1_TX #1	
PD3	BUSADC0Y BU-SADC0X OPA2_N	EBI_A07 #1 EBI_A16 #3	TIM4_CDTI2 TIM0_CC2 #2 TIM6_CC2 #6 WTIM1_CC1 #1 WTIM2_CC0 #5	CAN1_RX #2 US1_CS #1 LEU1_RX #2	ETM_TD1 #0 ETM_TD1 #2
PD8	BU_VIN	EBI_A12 #1	WTIM1_CC2 #2	US2_RTS #5	CMU_CLK1 #1 PRS_CH12 #2 ACMP2_O #0
PB7	LFXTAL_P		TIM0_CDTI0 #4 TIM1_CC0 #3	US0_TX #4 US1_CLK #0 US3_RX #2 US4_TX #0 U0_CTS #4	PRS_CH22 #0
PC3	VDAC0_OUT0ALT / OPA0_OUTALT #3 BUSACMP0Y BU-SACMP0X	EBI_AD10 #1 EBI_CS3 #2 EBI_BL1 #3 EBI_NANDREn #0	TIM0_CDTI1 #3 TIM2_CC1 #5 WTIM0_CC2 #7 LE-TIM1_OUT1 #3	ETH_TSUTMRTOG #2 CAN1_TX #0 US1_CLK #4 US2_RX #0	LES_CH3 PRS_CH11 #1
PC5	BUSACMP0Y BU-SACMP0X OPA0_N	EBI_AD12 #1 EBI_WEn #2 EBI_NANDWEn #0 EBI_A00 #3	TIM0_CC1 #5 LE-TIM0_OUT1 #3 PCNT1_S1IN #3	SDIO_WP #1 US2_CS #0 US4_CS #0 U0_RX #4 U1_RTS #4 I2C1_SCL #0	LES_CH5 PRS_CH19 #2
PA9	BUSAY BUSBX LCD_SEG37	EBI_AD15 #1 EBI_A03 #3 EBI_DTEN #0	TIM2_CC1 #0 TIM0_CC1 #6 WTIM2_CC0 #0 LE-TIM0_OUT1 #6	US2_CLK #2	PRS_CH9 #0
PB10	BUSBY BUSAX	EBI_BL0 #2 EBI_A01 #1 EBI_A04 #0 EBI_A10 #3	WTIM2_CC1 #2 LE-TIM0_OUT1 #7	SDIO_CD #3 CAN0_TX #3 US1_RTS #0 US2_CTS #3 U1_RX #2	PRS_CH9 #2 ACMP1_O #6
PH0	BUSADC1Y BU-SADC1X	EBI_DCLK #2	WTIM2_CC2 #4	US0_CTS #6 LEU1_TX #5	
PH3	BUSADC1Y BU-SADC1X	EBI_HSNC #2	TIM6_CC1 #3	US1_RTS #6	
PH6	BUSADC1Y BU-SADC1X	EBI_A18 #2	TIM6_CDTI1 #3 WTIM2_CC2 #6	US4_CLK #4	
PH9	BUSACMP3Y BU-SACMP3X	EBI_A21 #2	TIM6_CC1 #4 WTIM1_CC1 #6 WTIM2_CC2 #7	US4_RTS #4	
PH12	BUSACMP3Y BU-SACMP3X	EBI_A24 #2	TIM5_CC2 #1 WTIM1_CC0 #7	US5_CLK #3 U1_RX #5 I2C1_SCL #5	

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PH14	BUSACMP3Y BU-SACMP3X	EBI_A26 #2	TIM5_CC1 #2 WTIM1_CC2 #7 PCNT2_S0IN #7	US5_CTS #3 U1_RTS #5 I2C1_SCL #6	
PH15	BUSACMP3Y BU-SACMP3X	EBI_A27 #2	TIM5_CC2 #2 WTIM1_CC3 #7 PCNT2_S1IN #6	US5_RTS #3	
PD2	BUSADC0Y BU-SADC0X	EBI_A06 #1 EBI_A15 #3 EBI_A27 #0	TIM0_CC1 #2 TIM6_CC1 #6 WTIM1_CC0 #1	US1_CLK #1 LEU1_TX #2	DBG_SWO #3
PD7	BUSADC0Y BU-SADC0X ADC0_EXTN ADC1_EXTN OPA1_N	EBI_A11 #1 EBI_A20 #3	TIM1_CC1 #4 WTIM1_CC1 #2 LE-TIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 US3_CLK #1 U0_TX #6 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 ACMP1_O #2 ETM_TCLK #0
PB8	LFXTAL_N		TIM0_CDTI1 #4 TIM1_CC1 #3	US0_RX #4 US1_CS #0 US4_RX #0 U0_RTS #4	CMU_CLKI0 #2 PRS_CH23 #0
PC4	BUSACMP0Y BU-SACMP0X OPA0_P	EBI_AD11 #1 EBI_ALE #2 EBI_NANDREn #3 EBI_A26 #0	TIM0_CC0 #5 TIM0_CDTI2 #3 TIM2_CC2 #5 LE-TIM0_OUT0 #3 PCNT1_S0IN #3	SDIO_CD #1 US2_CLK #0 US4_CLK #0 U0_TX #4 U1_CTS #4 I2C1_SDA #0	LES_CH4 PRS_CH18 #2 GPIO_EM4WU6
PA7	BUSAY BUSBX LCD_SEG35	EBI_AD13 #1 EBI_A01 #3 EBI_CSTFT #0	TIM0_CC2 #5 LE-TIM1_OUT0 #0 PCNT1_S0IN #4	US2_TX #2 US4_CTS #0 US5_RX #1	PRS_CH7 #1
PA10	BUSBY BUSAX LCD_SEG38	EBI_CS0 #1 EBI_A04 #3 EBI_VSNC #0	TIM2_CC2 #0 TIM0_CC2 #6 WTIM2_CC1 #0	US2_CS #2	PRS_CH10 #0
PA12	BUSBY BUSAX	EBI_CS2 #1 EBI_REn #2 EBI_A00 #0 EBI_A06 #3	TIM2_CC0 #1 WTIM0_CDTI0 #2 WTIM2_CC0 #1 LE-TIM1_OUT0 #2 PCNT1_S0IN #5	CAN1_RX #5 US0_CLK #5 US2_RTS #2	CMU_CLK0 #5 PRS_CH12 #0 ACMP1_O #3
PA14	BUSBY BUSAX LCD_BEXT	EBI_REn #1 EBI_A02 #0 EBI_A08 #3	TIM2_CC2 #1 WTIM0_CDTI2 #2 WTIM2_CC2 #1 LE-TIM1_OUT1 #2	US1_TX #6 US2_RX #3 US3_RTS #2	PRS_CH14 #0 ACMP1_O #4
PB11	BUSAY BUSBX VDAC0_OUT0 / OPA0_OUT IDAC0_OUT	EBI_BL1 #2 EBI_A02 #1 EBI_A11 #3	TIM0_CDTI2 #4 TIM1_CC2 #3 WTIM2_CC2 #2 LE-TIM0_OUT0 #1 PCNT0_S1IN #7 PCNT1_S0IN #6	US0_CTS #5 US1_CLK #5 US2_CS #3 US5_CLK #0 U1_CTS #2 I2C1_SDA #1	CMU_CLK1 #5 CMU_CLKI0 #7 PRS_CH21 #2 ACMP0_O #3 GPIO_EM4WU7
PH1	BUSADC1Y BU-SADC1X	EBI_DTEN #2		US0_RTS #6 LEU1_RX #5	
PH4	BUSADC1Y BU-SADC1X	EBI_A16 #2	TIM6_CC2 #3 WTIM2_CC0 #6	US4_TX #4	
PH7	BUSADC1Y BU-SADC1X	EBI_A19 #2	TIM6_CDTI2 #3 WTIM2_CC0 #7	US4_CS #4	
PH10	BUSACMP3Y BU-SACMP3X	EBI_A22 #2	TIM6_CC2 #4 WTIM1_CC2 #6	US5_TX #3	

GPIO Name	Pin Alternate Functionality / Description				
	Analog	EBI	Timers	Communication	Other
PB13	BUSAY BUSBX HFXTAL_P		TIM6_CC0 #5 WTIM1_CC0 #0 PCNT2_S0IN #2	US0_CLK #4 US1_CTS #5 US5_CS #0 LEU0_TX #1	CMU_CLKI0 #3 PRS_CH7 #0
PB14	BUSBY BUSAX HFXTAL_N		TIM6_CC1 #5 WTIM1_CC1 #0 PCNT2_S1IN #2	US0_CS #4 US1_RTS #5 US5_CTS #0 LEU0_RX #1	PRS_CH6 #1
PD1	VDAC0_OUT1ALT / OPA1_OUTALT #4 BUSADC0Y BU-SADC0X OPA3_OUT	EBI_A05 #1 EBI_A14 #3	TIM4_CDTI1 TIM0_CC0 #2 TIM6_CC0 #6 WTIM1_CC3 #0 PCNT2_S1IN #0	CAN0_TX #2 US1_RX #1	DBG_SWO #2
PD6	BUSADC0Y BU-SADC0X ADC0_EXTP VDAC0_EXT ADC1_EXTP OPA1_P	EBI_A10 #1 EBI_A19 #3	TIM1_CC0 #4 TIM6_CC2 #7 WTIM0_CDTI2 #4 WTIM1_CC0 #2 LE-TIM0_OUT0 #0 PCNT0_S0IN #3	US0_RTS #5 US1_RX #2 US2_CTS #5 US3_CTS #2 U0_RTS #5 I2C0_SDA #1	CMU_CLK2 #2 LES_ALTEX0 PRS_CH5 #2 ACMP0_O #2 ETM_TD0 #0

5.4 Alternate Functionality Overview

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings and the associated GPIO pin. Refer to 5.3 GPIO Functionality Table for a list of functions available on each GPIO pin.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.4. Alternate Functionality Overview

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
ACMP0_O	0: PE13 1: PE2 2: PD6 3: PB11	4: PA6 5: PB0 6: PB2 7: PB3	Analog comparator ACMP0, digital output.
ACMP1_O	0: PF2 1: PE3 2: PD7 3: PA12	4: PA14 5: PB9 6: PB10 7: PA5	Analog comparator ACMP1, digital output.
ACMP2_O	0: PD8 1: PE0 2: PE1 3: PI0	4: PI1 5: PI2	Analog comparator ACMP2, digital output.
ACMP3_O	0: PF0 1: PC15 2: PC14 3: PC13	4: PI4 5: PI5	Analog comparator ACMP3, digital output.
ADC0_EXTN	0: PD7		Analog to digital converter ADC0 external reference input negative pin.
ADC0_EXTP	0: PD6		Analog to digital converter ADC0 external reference input positive pin.
ADC1_EXTN	0: PD7		Analog to digital converter ADC1 external reference input negative pin.
ADC1_EXTP	0: PD6		Analog to digital converter ADC1 external reference input positive pin.
BOOT_RX	0: PF1		Bootloader RX.
BOOT_TX	0: PF0		Bootloader TX.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
BU_STAT	0: PE3		Backup Power Domain status, whether or not the system is in backup mode.
BU_VIN	0: PD8		Battery input for Backup Power Domain.
BU_VOUT	0: PE2		Power output for Backup Power Domain.
CAN0_RX	0: PC0 1: PF0 2: PD0 3: PB9	4: PG8 5: PD14 6: PE0 7: PI12	CAN0 RX.
CAN0_TX	0: PC1 1: PF2 2: PD1 3: PB10	4: PG9 5: PD15 6: PE1 7: PI13	CAN0 TX.
CAN1_RX	0: PC2 1: PF1 2: PD3 3: PC9	4: PC12 5: PA12 6: PG10 7: PI14	CAN1 RX.
CAN1_TX	0: PC3 1: PF3 2: PD4 3: PC10	4: PC11 5: PA13 6: PG11 7: PI15	CAN1 TX.
CMU_CLK0	0: PA2 1: PC12 2: PD7 3: PG2	4: PF2 5: PA12	Clock Management Unit, clock output number 0.
CMU_CLK1	0: PA1 1: PD8 2: PE12 3: PG1	4: PF3 5: PB11	Clock Management Unit, clock output number 1.
CMU_CLK2	0: PA0 1: PA3 2: PD6 3: PG0	4: PA3 5: PD10	Clock Management Unit, clock output number 2.
CMU_CLKI0	0: PD4 1: PA3 2: PB8 3: PB13	4: PE1 5: PD10 6: PE12 7: PB11	Clock Management Unit, clock output number I0.
DBG_SWCLKTCK	0: PF0		Debug-interface Serial Wire clock input and JTAG Test Clock. Note that this function is enabled to the pin out of reset, and has a built-in pull down.
DBG_SWDIOTMS	0: PF1		Debug-interface Serial Wire data input / output and JTAG Test Mode Select. Note that this function is enabled to the pin out of reset, and has a built-in pull up.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
DBG_SWO	0: PF2 1: PC15 2: PD1 3: PD2		Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
DBG_TDI	0: PF5		Debug-interface JTAG Test Data In. Note that this function becomes available after the first valid JTAG command is received, and has a built-in pull up when JTAG is active.
DBG_TDO	0: PF2		Debug-interface JTAG Test Data Out. Note that this function becomes available after the first valid JTAG command is received.
EBI_A00	0: PA12 1: PB9 2: PE0 3: PC5		External Bus Interface (EBI) address output pin 00.
EBI_A01	0: PA13 1: PB10 2: PE1 3: PA7		External Bus Interface (EBI) address output pin 01.
EBI_A02	0: PA14 1: PB11 2: PI0 3: PA8		External Bus Interface (EBI) address output pin 02.
EBI_A03	0: PB9 1: PB12 2: PI1 3: PA9		External Bus Interface (EBI) address output pin 03.
EBI_A04	0: PB10 1: PD0 2: PI2 3: PA10		External Bus Interface (EBI) address output pin 04.
EBI_A05	0: PC6 1: PD1 2: PI3 3: PA11		External Bus Interface (EBI) address output pin 05.
EBI_A06	0: PC7 1: PD2 2: PI4 3: PA12		External Bus Interface (EBI) address output pin 06.
EBI_A07	0: PE0 1: PD3 2: PI5 3: PA13		External Bus Interface (EBI) address output pin 07.
EBI_A08	0: PE1 1: PD4 2: PC8 3: PA14		External Bus Interface (EBI) address output pin 08.
EBI_A09	0: PE2 1: PD5 2: PC9 3: PB9		External Bus Interface (EBI) address output pin 09.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
EBI_A10	0: PE3 1: PD6 2: PC10 3: PB10		External Bus Interface (EBI) address output pin 10.
EBI_A11	0: PE4 1: PD7 2: PI6 3: PB11		External Bus Interface (EBI) address output pin 11.
EBI_A12	0: PE5 1: PD8 2: PI7 3: PB12		External Bus Interface (EBI) address output pin 12.
EBI_A13	0: PE6 1: PC7 2: PI8 3: PD0		External Bus Interface (EBI) address output pin 13.
EBI_A14	0: PE7 1: PE2 2: PI9 3: PD1		External Bus Interface (EBI) address output pin 14.
EBI_A15	0: PC8 1: PE3 2: PI10 3: PD2		External Bus Interface (EBI) address output pin 15.
EBI_A16	0: PB0 1: PE4 2: PH4 3: PD3		External Bus Interface (EBI) address output pin 16.
EBI_A17	0: PB1 1: PE5 2: PH5 3: PD4		External Bus Interface (EBI) address output pin 17.
EBI_A18	0: PB2 1: PE6 2: PH6 3: PD5		External Bus Interface (EBI) address output pin 18.
EBI_A19	0: PB3 1: PE7 2: PH7 3: PD6		External Bus Interface (EBI) address output pin 19.
EBI_A20	0: PB4 1: PC8 2: PH8 3: PD7		External Bus Interface (EBI) address output pin 20.
EBI_A21	0: PB5 1: PC9 2: PH9 3: PC7		External Bus Interface (EBI) address output pin 21.
EBI_A22	0: PB6 1: PC10 2: PH10 3: PE4		External Bus Interface (EBI) address output pin 22.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
EBI_A23	0: PC0 1: PC11 2: PH11 3: PE5		External Bus Interface (EBI) address output pin 23.
EBI_A24	0: PC1 1: PF0 2: PH12 3: PE6		External Bus Interface (EBI) address output pin 24.
EBI_A25	0: PC2 1: PF1 2: PH13 3: PE7		External Bus Interface (EBI) address output pin 25.
EBI_A26	0: PC4 1: PF2 2: PH14 3: PC8		External Bus Interface (EBI) address output pin 26.
EBI_A27	0: PD2 1: PF5 2: PH15 3: PC9		External Bus Interface (EBI) address output pin 27.
EBI_AD00	0: PE8 1: PB0 2: PG0		External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	0: PE9 1: PB1 2: PG1		External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	0: PE10 1: PB2 2: PG2		External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	0: PE11 1: PB3 2: PG3		External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	0: PE12 1: PB4 2: PG4		External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	0: PE13 1: PB5 2: PG5		External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	0: PE14 1: PB6 2: PG6		External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	0: PE15 1: PC0 2: PG7		External Bus Interface (EBI) address and data input / output pin 07.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
EBI_AD08	0: PA15 1: PC1 2: PG8		External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	0: PA0 1: PC2 2: PG9		External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	0: PA1 1: PC3 2: PG10		External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	0: PA2 1: PC4 2: PG11		External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	0: PA3 1: PC5 2: PG12		External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	0: PA4 1: PA7 2: PG13		External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	0: PA5 1: PA8 2: PG14		External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	0: PA6 1: PA9 2: PG15		External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	0: PF3 1: PB9 2: PC4 3: PB5	4: PC11 5: PC11	External Bus Interface (EBI) Address Latch Enable output.
EBI_ARDY	0: PF2 1: PD13 2: PB15 3: PB4	4: PC13 5: PF10	External Bus Interface (EBI) Hardware Ready Control input.
EBI_BL0	0: PF6 1: PF8 2: PB10 3: PC1	4: PF6 5: PF6	External Bus Interface (EBI) Byte Lane/Enable pin 0.
EBI_BL1	0: PF7 1: PF9 2: PB11 3: PC3	4: PF7 5: PF7	External Bus Interface (EBI) Byte Lane/Enable pin 1.
EBI_CS0	0: PD9 1: PA10 2: PC0 3: PB0	4: PE8	External Bus Interface (EBI) Chip Select output 0.

Alternate Functionality	LOCATION 0 - 3	LOCATION 4 - 7	Description
EBI_CS1	0: PD10 1: PA11 2: PC1 3: PB1	4: PE9	External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	0: PD11 1: PA12 2: PC2 3: PB2	4: PE10	External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	0: PD12 1: PB15 2: PC3 3: PB3	4: PE11	External Bus Interface (EBI) Chip Select output 3.
EBI_CSTFT	0: PA7 1: PF6 2: PB12 3: PA0		External Bus Interface (EBI) Chip Select output TFT.
EBI_DCLK	0: PA8 1: PF7 2: PH0 3: PA1		External Bus Interface (EBI) TFT Dot Clock pin.
EBI_DTEN	0: PA9 1: PD9 2: PH1 3: PA2		External Bus Interface (EBI) TFT Data Enable pin.
EBI_HSNC	0: PA11 1: PD11 2: PH3 3: PA4		External Bus Interface (EBI) TFT Horizontal Synchronization pin.
EBI_NANDREn	0: PC3 1: PD15 2: PB9 3: PC4	4: PC15 5: PF12	External Bus Interface (EBI) NAND Read Enable output.
EBI_NANDWEn	0: PC5 1: PD14 2: PA13 3: PC2	4: PC14 5: PF11	External Bus Interface (EBI) NAND Write Enable output.
EBI_REn	0: PF5 1: PA14 2: PA12 3: PC0	4: PF9 5: PF5	External Bus Interface (EBI) Read Enable output.
EBI_VSNC	0: PA10 1: PD10 2: PH2 3: PA3		External Bus Interface (EBI) TFT Vertical Synchronization pin.
EBI_WEn	0: PF4 1: PA13 2: PC5 3: PB6	4: PF8 5: PF4	External Bus Interface (EBI) Write Enable output.
ETH_MDC	0: PB4 1: PD14 2: PC1 3: PA6		Ethernet Management Data Clock.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
ETH_MDIO	0: PB3 1: PD13 2: PC0 3: PA15		Ethernet Management Data I/O.
ETH_MIICOL	0: PB2 1: PG15 2: PB4		Ethernet MII Collision Detect.
ETH_MIICRS	0: PB1 1: PG14 2: PB3		Ethernet MII Carrier Sense.
ETH_MIIRXCLK	0: PA15 1: PG7 2: PD12		Ethernet MII Receive Clock.
ETH_MIIRXD0	0: PE12 1: PG11 2: PF9		Ethernet MII Receive Data Bit 0.
ETH_MIIRXD1	0: PE13 1: PG10 2: PD9		Ethernet MII Receive Data Bit 1.
ETH_MIIRXD2	0: PE14 1: PG9 2: PD10		Ethernet MII Receive Data Bit 2.
ETH_MIIRXD3	0: PE15 1: PG8 2: PD11		Ethernet MII Receive Data Bit 3.
ETH_MIIRXDV	0: PE11 1: PG12 2: PF8		Ethernet MII Receive Data Valid.
ETH_MIIRXER	0: PE10 1: PG13 2: PF7		Ethernet MII Receive Error.
ETH_MIITXCLK	0: PA0 1: PG0		Ethernet MII Transmit Clock.
ETH_MIITXD0	0: PA4 1: PG4		Ethernet MII Transmit Data Bit 0.
ETH_MIITXD1	0: PA3 1: PG3		Ethernet MII Transmit Data Bit 1.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
ETH_MIITXD2	0: PA2 1: PG2		Ethernet MII Transmit Data Bit 2.
ETH_MIITXD3	0: PA1 1: PG1		Ethernet MII Transmit Data Bit 3.
ETH_MIITXEN	0: PA5 1: PG5		Ethernet MII Transmit Enable.
ETH_MIITXER	0: PA6 1: PG6		Ethernet MII Transmit Error.
ETH_RMIICRSDV	0: PA4 1: PD11		Ethernet RMII Carrier Sense / Data Valid.
ETH_RMIIREFCLK	0: PA3 1: PD10		Ethernet RMII Reference Clock.
ETH_RMIIRXD0	0: PA2 1: PD9		Ethernet RMII Receive Data Bit 0.
ETH_RMIIRXD1	0: PA1 1: PF9		Ethernet RMII Receive Data Bit 1.
ETH_RMIIRXER	0: PA5 1: PD12		Ethernet RMII Receive Error.
ETH_RMIITXD0	0: PE15 1: PF7		Ethernet RMII Transmit Data Bit 0.
ETH_RMIITXD1	0: PE14 1: PF6		Ethernet RMII Transmit Data Bit 1.
ETH_RMIITXEN	0: PA0 1: PF8		Ethernet RMII Transmit Enable.
ETH_TSUEXTCLK	0: PB5 1: PD15 2: PC2 3: PF8		Ethernet IEEE1588 External Reference Clock.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
ETH_TSUTMR-TOG	0: PB6 1: PB15 2: PC3 3: PF9		Ethernet IEEE1588 Timer Toggle.
ETM_TCLK	0: PD7 1: PF8 2: PC6 3: PA6	4: PE11 5: PG15	Embedded Trace Module ETM clock .
ETM_TD0	0: PD6 1: PF9 2: PC7 3: PA2	4: PE12 5: PG14	Embedded Trace Module ETM data 0.
ETM_TD1	0: PD3 1: PD13 2: PD3 3: PA3	4: PE13 5: PG13	Embedded Trace Module ETM data 1.
ETM_TD2	0: PD4 1: PB15 2: PD4 3: PA4	4: PE14 5: PG12	Embedded Trace Module ETM data 2.
ETM_TD3	0: PD5 1: PF3 2: PD5 3: PA5	4: PE15 5: PG11	Embedded Trace Module ETM data 3.
GPIO_EM4WU0	0: PA0		Pin can be used to wake the system up from EM4
GPIO_EM4WU1	0: PA6		Pin can be used to wake the system up from EM4
GPIO_EM4WU2	0: PC9		Pin can be used to wake the system up from EM4
GPIO_EM4WU3	0: PF1		Pin can be used to wake the system up from EM4
GPIO_EM4WU4	0: PF2		Pin can be used to wake the system up from EM4
GPIO_EM4WU5	0: PE13		Pin can be used to wake the system up from EM4
GPIO_EM4WU6	0: PC4		Pin can be used to wake the system up from EM4

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
GPIO_EM4WU7	0: PB11		Pin can be used to wake the system up from EM4
GPIO_EM4WU8	0: PF8		Pin can be used to wake the system up from EM4
GPIO_EM4WU9	0: PE10		Pin can be used to wake the system up from EM4
HFXTAL_N	0: PB14		High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	0: PB13		High Frequency Crystal positive pin.
I2C0_SCL	0: PA1 1: PD7 2: PC7 3: PD15	4: PC1 5: PF1 6: PE13 7: PE5	I2C0 Serial Clock Line input / output.
I2C0_SDA	0: PA0 1: PD6 2: PC6 3: PD14	4: PC0 5: PF0 6: PE12 7: PE4	I2C0 Serial Data input / output.
I2C1_SCL	0: PC5 1: PB12 2: PE1 3: PD5	4: PF2 5: PH12 6: PH14 7: PI3	I2C1 Serial Clock Line input / output.
I2C1_SDA	0: PC4 1: PB11 2: PE0 3: PD4	4: PC11 5: PH11 6: PH13 7: PI2	I2C1 Serial Data input / output.
I2C2_SCL	0: PF5 1: PC15 2: PF11 3: PF12	4: PF14 5: PF3 6: PC13 7: PI5	I2C2 Serial Clock Line input / output.
I2C2_SDA	0: PE8 1: PC14 2: PF10 3: PF4	4: PF13 5: PF15 6: PC12 7: PI4	I2C2 Serial Data input / output.
IDAC0_OUT	0: PB11		IDAC0 output.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LCD_BEXT	0: PA14		LCD external supply bypass in step down or charge pump mode. If using the LCD in step-down or charge pump mode, a 1 uF (minimum) capacitor between this pin and VSS is required. To reduce supply ripple, a larger capcitor of approximately 1000 times the total LCD segment capacitance may be used. If using the LCD with the internal supply source, this pin may be left unconnected or used as a GPIO.
LCD_COM0	0: PE4		LCD driver common line number 0.
LCD_COM1	0: PE5		LCD driver common line number 1.
LCD_COM2	0: PE6		LCD driver common line number 2.
LCD_COM3	0: PE7		LCD driver common line number 3.
LCD_SEG0	0: PF2		LCD segment line 0.
LCD_SEG1	0: PF3		LCD segment line 1.
LCD_SEG2	0: PF4		LCD segment line 2.
LCD_SEG3	0: PF5		LCD segment line 3.
LCD_SEG4	0: PE8		LCD segment line 4.
LCD_SEG5	0: PE9		LCD segment line 5.
LCD_SEG6	0: PE10		LCD segment line 6.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LCD_SEG7	0: PE11		LCD segment line 7.
LCD_SEG8	0: PE12		LCD segment line 8.
LCD_SEG9	0: PE13		LCD segment line 9.
LCD_SEG10	0: PE14		LCD segment line 10.
LCD_SEG11	0: PE15		LCD segment line 11.
LCD_SEG12	0: PA15		LCD segment line 12.
LCD_SEG13	0: PA0		LCD segment line 13.
LCD_SEG14	0: PA1		LCD segment line 14.
LCD_SEG15	0: PA2		LCD segment line 15.
LCD_SEG16	0: PA3		LCD segment line 16.
LCD_SEG17	0: PA4		LCD segment line 17.
LCD_SEG18	0: PA5		LCD segment line 18.
LCD_SEG19	0: PA6		LCD segment line 19.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LCD_SEG20 / LCD_COM4	0: PB3		LCD segment line 20. This pin may also be used as LCD COM line 4
LCD_SEG21 / LCD_COM5	0: PB4		LCD segment line 21. This pin may also be used as LCD COM line 5
LCD_SEG22 / LCD_COM6	0: PB5		LCD segment line 22. This pin may also be used as LCD COM line 6
LCD_SEG23 / LCD_COM7	0: PB6		LCD segment line 23. This pin may also be used as LCD COM line 7
LCD_SEG24	0: PF6		LCD segment line 24.
LCD_SEG25	0: PF7		LCD segment line 25.
LCD_SEG26	0: PF8		LCD segment line 26.
LCD_SEG27	0: PF9		LCD segment line 27.
LCD_SEG28	0: PD9		LCD segment line 28.
LCD_SEG29	0: PD10		LCD segment line 29.
LCD_SEG30	0: PD11		LCD segment line 30.
LCD_SEG31	0: PD12		LCD segment line 31.
LCD_SEG32	0: PB0		LCD segment line 32.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LCD_SEG33	0: PB1		LCD segment line 33.
LCD_SEG34	0: PB2		LCD segment line 34.
LCD_SEG35	0: PA7		LCD segment line 35.
LCD_SEG36	0: PA8		LCD segment line 36.
LCD_SEG37	0: PA9		LCD segment line 37.
LCD_SEG38	0: PA10		LCD segment line 38.
LCD_SEG39	0: PA11		LCD segment line 39.
LES_ALTEX0	0: PD6		LESENSE alternate excite output 0.
LES_ALTEX1	0: PD7		LESENSE alternate excite output 1.
LES_ALTEX2	0: PA3		LESENSE alternate excite output 2.
LES_ALTEX3	0: PA4		LESENSE alternate excite output 3.
LES_ALTEX4	0: PA5		LESENSE alternate excite output 4.
LES_ALTEX5	0: PE11		LESENSE alternate excite output 5.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LES_ALTEX6	0: PE12		LESENSE alternate excite output 6.
LES_ALTEX7	0: PE13		LESENSE alternate excite output 7.
LES_CH0	0: PC0		LESENSE channel 0.
LES_CH1	0: PC1		LESENSE channel 1.
LES_CH2	0: PC2		LESENSE channel 2.
LES_CH3	0: PC3		LESENSE channel 3.
LES_CH4	0: PC4		LESENSE channel 4.
LES_CH5	0: PC5		LESENSE channel 5.
LES_CH6	0: PC6		LESENSE channel 6.
LES_CH7	0: PC7		LESENSE channel 7.
LES_CH8	0: PC8		LESENSE channel 8.
LES_CH9	0: PC9		LESENSE channel 9.
LES_CH10	0: PC10		LESENSE channel 10.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LES_CH11	0: PC11		LESENSE channel 11.
LES_CH12	0: PC12		LESENSE channel 12.
LES_CH13	0: PC13		LESENSE channel 13.
LES_CH14	0: PC14		LESENSE channel 14.
LES_CH15	0: PC15		LESENSE channel 15.
LETIM0_OUT0	0: PD6 1: PB11 2: PF0 3: PC4	4: PE12 5: PC14 6: PA8 7: PB9	Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	0: PD7 1: PB12 2: PF1 3: PC5	4: PE13 5: PC15 6: PA9 7: PB10	Low Energy Timer LETIM0, output channel 1.
LETIM1_OUT0	0: PA7 1: PA11 2: PA12 3: PC2	4: PB5 5: PB2 6: PG0 7: PG2	Low Energy Timer LETIM1, output channel 0.
LETIM1_OUT1	0: PA6 1: PA13 2: PA14 3: PC3	4: PB6 5: PB1 6: PG1 7: PG3	Low Energy Timer LETIM1, output channel 1.
LEU0_RX	0: PD5 1: PB14 2: PE15 3: PF1	4: PA0 5: PC15	LEUART0 Receive input.
LEU0_TX	0: PD4 1: PB13 2: PE14 3: PF0	4: PF2 5: PC14	LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	0: PC7 1: PA6 2: PD3 3: PB1	4: PB5 5: PH1	LEUART1 Receive input.
LEU1_TX	0: PC6 1: PA5 2: PD2 3: PB0	4: PB4 5: PH0	LEUART1 Transmit output. Also used as receive input in half duplex communication.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
LFXTAL_N	0: PB8		Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	0: PB7		Low Frequency Crystal (typically 32.768 kHz) positive pin.
OPA0_N	0: PC5		Operational Amplifier 0 external negative input.
OPA0_P	0: PC4		Operational Amplifier 0 external positive input.
OPA1_N	0: PD7		Operational Amplifier 1 external negative input.
OPA1_P	0: PD6		Operational Amplifier 1 external positive input.
OPA2_N	0: PD3		Operational Amplifier 2 external negative input.
OPA2_OUT	0: PD5		Operational Amplifier 2 output.
OPA2_OUTALT	0: PD0		Operational Amplifier 2 alternative output.
OPA2_P	0: PD4		Operational Amplifier 2 external positive input.
OPA3_N	0: PC7		Operational Amplifier 3 external negative input.
OPA3_OUT	0: PD1		Operational Amplifier 3 output.
OPA3_P	0: PC6		Operational Amplifier 3 external positive input.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
PCNT0_S0IN	0: PC13 1: PE0 2: PC0 3: PD6	4: PA0 5: PB0 6: PB5 7: PB12	Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	0: PC14 1: PE1 2: PC1 3: PD7	4: PA1 5: PB1 6: PB6 7: PB11	Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	0: PA5 1: PB3 2: PD15 3: PC4	4: PA7 5: PA12 6: PB11 7: PG14	Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	0: PA6 1: PB4 2: PB0 3: PC5	4: PA8 5: PA13 6: PB12 7: PG15	Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	0: PD0 1: PE8 2: PB13 3: PF10	4: PC12 5: PI2 6: PI0 7: PH14	Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	0: PD1 1: PE9 2: PB14 3: PF11	4: PC13 5: PI1 6: PH15 7: PH13	Pulse Counter PCNT2 input number 1.
PRS_CH0	0: PA0 1: PF3 2: PC14 3: PF2		Peripheral Reflex System PRS, channel 0.
PRS_CH1	0: PA1 1: PF4 2: PC15 3: PE12		Peripheral Reflex System PRS, channel 1.
PRS_CH2	0: PC0 1: PF5 2: PE10 3: PE13		Peripheral Reflex System PRS, channel 2.
PRS_CH3	0: PC1 1: PE8 2: PE11 3: PA0		Peripheral Reflex System PRS, channel 3.
PRS_CH4	0: PC8 1: PB0 2: PF1		Peripheral Reflex System PRS, channel 4.
PRS_CH5	0: PC9 1: PB1 2: PD6		Peripheral Reflex System PRS, channel 5.
PRS_CH6	0: PA6 1: PB14 2: PE6		Peripheral Reflex System PRS, channel 6.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
PRS_CH7	0: PB13 1: PA7 2: PE7		Peripheral Reflex System PRS, channel 7.
PRS_CH8	0: PA8 1: PA2 2: PE9		Peripheral Reflex System PRS, channel 8.
PRS_CH9	0: PA9 1: PA3 2: PB10		Peripheral Reflex System PRS, channel 9.
PRS_CH10	0: PA10 1: PC2 2: PD4		Peripheral Reflex System PRS, channel 10.
PRS_CH11	0: PA11 1: PC3 2: PD5		Peripheral Reflex System PRS, channel 11.
PRS_CH12	0: PA12 1: PB6 2: PD8		Peripheral Reflex System PRS, channel 12.
PRS_CH13	0: PA13 1: PB9 2: PE14		Peripheral Reflex System PRS, channel 13.
PRS_CH14	0: PA14 1: PC6 2: PE15		Peripheral Reflex System PRS, channel 14.
PRS_CH15	0: PA15 1: PC7 2: PF0		Peripheral Reflex System PRS, channel 15.
PRS_CH16	0: PA4 1: PB12 2: PE4		Peripheral Reflex System PRS, channel 16.
PRS_CH17	0: PA5 1: PB15 2: PE5		Peripheral Reflex System PRS, channel 17.
PRS_CH18	0: PB2 1: PC10 2: PC4		Peripheral Reflex System PRS, channel 18.
PRS_CH19	0: PB3 1: PC11 2: PC5		Peripheral Reflex System PRS, channel 19.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
PRS_CH20	0: PB4 1: PC12 2: PE2		Peripheral Reflex System PRS, channel 20.
PRS_CH21	0: PB5 1: PC13 2: PB11		Peripheral Reflex System PRS, channel 21.
PRS_CH22	0: PB7 1: PE0 2: PF6		Peripheral Reflex System PRS, channel 22.
PRS_CH23	0: PB8 1: PE1 2: PF7		Peripheral Reflex System PRS, channel 23.
QSPI0_CS0	0: PF7 1: PA0 2: PG9		Quad SPI 0 Chip Select 0.
QSPI0_CS1	0: PF8 1: PA1 2: PG10		Quad SPI 0 Chip Select 1.
QSPI0_DQ0	0: PD9 1: PA2 2: PG1		Quad SPI 0 Data 0.
QSPI0_DQ1	0: PD10 1: PA3 2: PG2		Quad SPI 0 Data 1.
QSPI0_DQ2	0: PD11 1: PA4 2: PG3		Quad SPI 0 Data 2.
QSPI0_DQ3	0: PD12 1: PA5 2: PG4		Quad SPI 0 Data 3.
QSPI0_DQ4	0: PE8 1: PB3 2: PG5		Quad SPI 0 Data 4.
QSPI0_DQ5	0: PE9 1: PB4 2: PG6		Quad SPI 0 Data 5.
QSPI0_DQ6	0: PE10 1: PB5 2: PG7		Quad SPI 0 Data 6.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
QSPI0_DQ7	0: PE11 1: PB6 2: PG8		Quad SPI 0 Data 7.
QSPI0_DQS	0: PF9 1: PE15 2: PG11		Quad SPI 0 Data S.
QSPI0_SCLK	0: PF6 1: PE14 2: PG0		Quad SPI 0 Serial Clock.
SDIO_CD	0: PF8 1: PC4 2: PA6 3: PB10		SDIO Card Detect.
SDIO_CLK	0: PE13 1: PE14		SDIO Serial Clock.
SDIO_CMD	0: PE12 1: PE15		SDIO Command.
SDIO_DAT0	0: PE11 1: PA0		SDIO Data 0.
SDIO_DAT1	0: PE10 1: PA1		SDIO Data 1.
SDIO_DAT2	0: PE9 1: PA2		SDIO Data 2.
SDIO_DAT3	0: PE8 1: PA3		SDIO Data 3.
SDIO_DAT4	0: PD12 1: PA4		SDIO Data 4.
SDIO_DAT5	0: PD11 1: PA5		SDIO Data 5.
SDIO_DAT6	0: PD10 1: PB3		SDIO Data 6.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
SDIO_DAT7	0: PD9 1: PB4		SDIO Data 7.
SDIO_WP	0: PF9 1: PC5 2: PB15 3: PB9		SDIO Write Protect.
TIM0_CC0	0: PA0 1: PF6 2: PD1 3: PB6	4: PF0 5: PC4 6: PA8 7: PA1	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	0: PA1 1: PF7 2: PD2 3: PC0	4: PF1 5: PC5 6: PA9 7: PA0	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	0: PA2 1: PF8 2: PD3 3: PC1	4: PF2 5: PA7 6: PA10 7: PA13	Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	0: PA3 1: PC13 2: PF3 3: PC2	4: PB7	Timer 0 Complimentary Dead Time Insertion channel 0.
TIM0_CDTI1	0: PA4 1: PC14 2: PF4 3: PC3	4: PB8	Timer 0 Complimentary Dead Time Insertion channel 1.
TIM0_CDTI2	0: PA5 1: PC15 2: PF5 3: PC4	4: PB11	Timer 0 Complimentary Dead Time Insertion channel 2.
TIM1_CC0	0: PC13 1: PE10 2: PB0 3: PB7	4: PD6 5: PF2 6: PF13 7: PI6	Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	0: PC14 1: PE11 2: PB1 3: PB8	4: PD7 5: PF3 6: PF14 7: PI7	Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	0: PC15 1: PE12 2: PB2 3: PB11	4: PC13 5: PF4 6: PF15 7: PI8	Timer 1 Capture Compare input / output channel 2.
TIM1_CC3	0: PC12 1: PE13 2: PB3 3: PB12	4: PC14 5: PF12 6: PF5 7: PI9	Timer 1 Capture Compare input / output channel 3.
TIM2_CC0	0: PA8 1: PA12 2: PC8 3: PF2	4: PB6 5: PC2 6: PG8 7: PG5	Timer 2 Capture Compare input / output channel 0.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
TIM2_CC1	0: PA9 1: PA13 2: PC9 3: PE12	4: PC0 5: PC3 6: PG9 7: PG6	Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	0: PA10 1: PA14 2: PC10 3: PE13	4: PC1 5: PC4 6: PG10 7: PG7	Timer 2 Capture Compare input / output channel 2.
TIM2_CDTI0	0: PB0 1: PD13 2: PE8 3: PG0		Timer 2 Complimentary Dead Time Insertion channel 0.
TIM2_CDTI1	0: PB1 1: PD14 2: PE14 3: PG1		Timer 2 Complimentary Dead Time Insertion channel 1.
TIM2_CDTI2	0: PB2 1: PD15 2: PE15 3: PG2		Timer 2 Complimentary Dead Time Insertion channel 2.
TIM3_CC0	0: PE14 1: PE0 2: PE3 3: PE5	4: PA0 5: PA3 6: PA6 7: PD15	Timer 3 Capture Compare input / output channel 0.
TIM3_CC1	0: PE15 1: PE1 2: PE4 3: PE6	4: PA1 5: PA4 6: PD13 7: PB15	Timer 3 Capture Compare input / output channel 1.
TIM3_CC2	0: PA15 1: PE2 2: PE5 3: PE7	4: PA2 5: PA5 6: PD14 7: PB0	Timer 3 Capture Compare input / output channel 2.
TIM4_CC0	0: PF3 1: PF13 2: PF5 3: PI8	4: PF6 5: PF9 6: PD11 7: PE9	Timer 4 Capture Compare input / output channel 0.
TIM4_CC1	0: PF4 1: PF14 2: PI6 3: PI9	4: PF7 5: PD9 6: PD12 7: PE10	Timer 4 Capture Compare input / output channel 1.
TIM4_CC2	0: PF12 1: PF15 2: PI7 3: PI10	4: PF8 5: PD10 6: PE8 7: PE11	Timer 4 Capture Compare input / output channel 2.
TIM4_CDTI0	0: PD0		Timer 4 Complimentary Dead Time Insertion channel 0.
TIM4_CDTI1	0: PD1		Timer 4 Complimentary Dead Time Insertion channel 1.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
TIM4_CDTI2	0: PD3		Timer 4 Complimentary Dead Time Insertion channel 2.
TIM5_CC0	0: PE4 1: PE7 2: PH13 3: PI0	4: PC8 5: PC11 6: PC14 7: PF12	Timer 5 Capture Compare input / output channel 0.
TIM5_CC1	0: PE5 1: PH11 2: PH14 3: PI1	4: PC9 5: PC12 6: PF10 7: PF13	Timer 5 Capture Compare input / output channel 1.
TIM5_CC2	0: PE6 1: PH12 2: PH15 3: PI2	4: PC10 5: PC13 6: PF11 7: PF14	Timer 5 Capture Compare input / output channel 2.
TIM6_CC0	0: PG0 1: PG6 2: PG12 3: PH2	4: PH8 5: PB13 6: PD1 7: PD4	Timer 6 Capture Compare input / output channel 0.
TIM6_CC1	0: PG1 1: PG7 2: PG13 3: PH3	4: PH9 5: PB14 6: PD2 7: PD5	Timer 6 Capture Compare input / output channel 1.
TIM6_CC2	0: PG2 1: PG8 2: PG14 3: PH4	4: PH10 5: PD0 6: PD3 7: PD6	Timer 6 Capture Compare input / output channel 2.
TIM6_CDTI0	0: PG3 1: PG9 2: PE4 3: PH5		Timer 6 Complimentary Dead Time Insertion channel 0.
TIM6_CDTI1	0: PG4 1: PG10 2: PE5 3: PH6		Timer 6 Complimentary Dead Time Insertion channel 1.
TIM6_CDTI2	0: PG5 1: PG11 2: PE6 3: PH7		Timer 6 Complimentary Dead Time Insertion channel 2.
U0_CTS	0: PF8 1: PE2 2: PA5 3: PC13	4: PB7 5: PD5	UART0 Clear To Send hardware flow control input.
U0_RTS	0: PF9 1: PE3 2: PA6 3: PC12	4: PB8 5: PD6	UART0 Request To Send hardware flow control output.
U0_RX	0: PF7 1: PE1 2: PA4 3: PC15	4: PC5 5: PF2 6: PE4	UART0 Receive input.

Alternate	LOCATION		
Functionality	**0 - 3**	**4 - 7**	**Description**
U0_TX	0: PF6 1: PE0 2: PA3 3: PC14	4: PC4 5: PF1 6: PD7	UART0 Transmit output. Also used as receive input in half duplex communication.
U1_CTS	0: PC14 1: PF9 2: PB11 3: PE4	4: PC4 5: PH13	UART1 Clear To Send hardware flow control input.
U1_RTS	0: PC15 1: PF8 2: PB12 3: PE5	4: PC5 5: PH14	UART1 Request To Send hardware flow control output.
U1_RX	0: PC13 1: PF11 2: PB10 3: PE3	4: PE13 5: PH12	UART1 Receive input.
U1_TX	0: PC12 1: PF10 2: PB9 3: PE2	4: PE12 5: PH11	UART1 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	0: PE12 1: PE5 2: PC9 3: PC15	4: PB13 5: PA12 6: PG14	USART0 clock input / output.
US0_CS	0: PE13 1: PE4 2: PC8 3: PC14	4: PB14 5: PA13 6: PG15	USART0 chip select input / output.
US0_CTS	0: PE14 1: PE3 2: PC7 3: PC13	4: PB6 5: PB11 6: PH0	USART0 Clear To Send hardware flow control input.
US0_RTS	0: PE15 1: PE2 2: PC6 3: PC12	4: PB5 5: PD6 6: PH1	USART0 Request To Send hardware flow control output.
US0_RX	0: PE11 1: PE6 2: PC10 3: PE12	4: PB8 5: PC1 6: PG13	USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	0: PE10 1: PE7 2: PC11 3: PE13	4: PB7 5: PC0 6: PG12	USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	0: PB7 1: PD2 2: PF0 3: PC15	4: PC3 5: PB11 6: PE5	USART1 clock input / output.
US1_CS	0: PB8 1: PD3 2: PF1 3: PC14	4: PC0 5: PE4 6: PB2	USART1 chip select input / output.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
US1_CTS	0: PB9 1: PD4 2: PF3 3: PC6	4: PC12 5: PB13 6: PH2	USART1 Clear To Send hardware flow control input.
US1_RTS	0: PB10 1: PD5 2: PF4 3: PC7	4: PC13 5: PB14 6: PH3	USART1 Request To Send hardware flow control output.
US1_RX	0: PC1 1: PD1 2: PD6 3: PF7	4: PC2 5: PA0 6: PA2	USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	0: PC0 1: PD0 2: PD7 3: PF6	4: PC1 5: PF2 6: PA14	USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	0: PC4 1: PB5 2: PA9 3: PA15	4: PF8 5: PF2	USART2 clock input / output.
US2_CS	0: PC5 1: PB6 2: PA10 3: PB11	4: PF9 5: PF5	USART2 chip select input / output.
US2_CTS	0: PC1 1: PB12 2: PA11 3: PB10	4: PC12 5: PD6	USART2 Clear To Send hardware flow control input.
US2_RTS	0: PC0 1: PB15 2: PA12 3: PC14	4: PC13 5: PD8	USART2 Request To Send hardware flow control output.
US2_RX	0: PC3 1: PB4 2: PA8 3: PA14	4: PF7 5: PF1	USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	0: PC2 1: PB3 2: PA7 3: PA13	4: PF6 5: PF0	USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).
US3_CLK	0: PA2 1: PD7 2: PD4 3: PG8	4: PG2 5: PI14	USART3 clock input / output.
US3_CS	0: PA3 1: PE4 2: PC14 3: PC0	4: PG3 5: PI15	USART3 chip select input / output.
US3_CTS	0: PA4 1: PE5 2: PD6 3: PG10	4: PG4 5: PG9	USART3 Clear To Send hardware flow control input.

Alternate	LOCATION		
Functionality	**0 - 3**	**4 - 7**	**Description**
US3_RTS	0: PA5 1: PC1 2: PA14 3: PC15	4: PG5 5: PG11	USART3 Request To Send hardware flow control output.
US3_RX	0: PA1 1: PE7 2: PB7 3: PG7	4: PG1 5: PI13	USART3 Asynchronous Receive. USART3 Synchronous mode Master Input / Slave Output (MISO).
US3_TX	0: PA0 1: PE6 2: PB3 3: PG6	4: PG0 5: PI12	USART3 Asynchronous Transmit. Also used as receive input in half duplex communication. USART3 Synchronous mode Master Output / Slave Input (MOSI).
US4_CLK	0: PC4 1: PD11 2: PI2 3: PI8	4: PH6	USART4 clock input / output.
US4_CS	0: PC5 1: PD12 2: PI3 3: PI9	4: PH7	USART4 chip select input / output.
US4_CTS	0: PA7 1: PD13 2: PI4 3: PI10	4: PH8	USART4 Clear To Send hardware flow control input.
US4_RTS	0: PA8 1: PD14 2: PI5 3: PI11	4: PH9	USART4 Request To Send hardware flow control output.
US4_RX	0: PB8 1: PD10 2: PI1 3: PI7	4: PH5	USART4 Asynchronous Receive. USART4 Synchronous mode Master Input / Slave Output (MISO).
US4_TX	0: PB7 1: PD9 2: PI0 3: PI6	4: PH4	USART4 Asynchronous Transmit. Also used as receive input in half duplex communication. USART4 Synchronous mode Master Output / Slave Input (MOSI).
US5_CLK	0: PB11 1: PD13 2: PF13 3: PH12		USART5 clock input / output.
US5_CS	0: PB13 1: PD14 2: PF12 3: PH13		USART5 chip select input / output.
US5_CTS	0: PB14 1: PD15 2: PF11 3: PH14		USART5 Clear To Send hardware flow control input.
US5_RTS	0: PB12 1: PB15 2: PF10 3: PH15		USART5 Request To Send hardware flow control output.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
US5_RX	0: PE9 1: PA7 2: PB1 3: PH11		USART5 Asynchronous Receive. USART5 Synchronous mode Master Input / Slave Output (MISO).
US5_TX	0: PE8 1: PA6 2: PF15 3: PH10		USART5 Asynchronous Transmit. Also used as receive input in half duplex communication. USART5 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	0: PF10		USB D- pin.
USB_DP	0: PF11		USB D+ pin.
USB_ID	0: PF12		USB ID pin.
USB_VBUSEN	0: PF5		USB 5 V VBUS enable.
VDAC0_EXT	0: PD6		Digital to analog converter VDAC0 external reference input pin.
VDAC0_OUT0 / OPA0_OUT	0: PB11		Digital to Analog Converter DAC0 output channel number 0.
VDAC0_OUT0ALT / OPA0_OUTALT	0: PC0 1: PC1 2: PC2 3: PC3	4: PD0	Digital to Analog Converter DAC0 alternative output for channel 0.
VDAC0_OUT1 / OPA1_OUT	0: PB12		Digital to Analog Converter DAC0 output channel number 1.
VDAC0_OUT1ALT / OPA1_OUTALT	0: PC12 1: PC13 2: PC14 3: PC15	4: PD1	Digital to Analog Converter DAC0 alternative output for channel 1.
WTIM0_CC0	0: PE4 1: PA6 2: PG2 3: PG8	4: PC15 5: PB0 6: PB3 7: PC1	Wide timer 0 Capture Compare input / output channel 0.
WTIM0_CC1	0: PE5 1: PD13 2: PG3 3: PG9	4: PF0 5: PB1 6: PB4 7: PC2	Wide timer 0 Capture Compare input / output channel 1.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
WTIM0_CC2	0: PE6 1: PD14 2: PG4 3: PG10	4: PF1 5: PB2 6: PB5 7: PC3	Wide timer 0 Capture Compare input / output channel 2.
WTIM0_CDTI0	0: PE10 1: PD15 2: PA12 3: PG11	4: PD4	Wide timer 0 Complimentary Dead Time Insertion channel 0.
WTIM0_CDTI1	0: PE11 1: PG0 2: PA13 3: PG12	4: PD5	Wide timer 0 Complimentary Dead Time Insertion channel 1.
WTIM0_CDTI2	0: PE12 1: PG1 2: PA14 3: PG13	4: PD6	Wide timer 0 Complimentary Dead Time Insertion channel 2.
WTIM1_CC0	0: PB13 1: PD2 2: PD6 3: PC7	4: PE3 5: PE7 6: PH8 7: PH12	Wide timer 1 Capture Compare input / output channel 0.
WTIM1_CC1	0: PB14 1: PD3 2: PD7 3: PE0	4: PE4 5: PI0 6: PH9 7: PH13	Wide timer 1 Capture Compare input / output channel 1.
WTIM1_CC2	0: PD0 1: PD4 2: PD8 3: PE1	4: PE5 5: PI1 6: PH10 7: PH14	Wide timer 1 Capture Compare input / output channel 2.
WTIM1_CC3	0: PD1 1: PD5 2: PC6 3: PE2	4: PE6 5: PI2 6: PH11 7: PH15	Wide timer 1 Capture Compare input / output channel 3.
WTIM2_CC0	0: PA9 1: PA12 2: PB9 3: PB12	4: PG14 5: PD3 6: PH4 7: PH7	Wide timer 2 Capture Compare input / output channel 0.
WTIM2_CC1	0: PA10 1: PA13 2: PB10 3: PG12	4: PG15 5: PD4 6: PH5 7: PH8	Wide timer 2 Capture Compare input / output channel 1.
WTIM2_CC2	0: PA11 1: PA14 2: PB11 3: PG13	4: PH0 5: PD5 6: PH6 7: PH9	Wide timer 2 Capture Compare input / output channel 2.
WTIM3_CC0	0: PD9 1: PC8 2: PC11 3: PC14	4: PI3 5: PI6 6: PB6 7: PF13	Wide timer 3 Capture Compare input / output channel 0.
WTIM3_CC1	0: PD10 1: PC9 2: PC12 3: PF10	4: PI4 5: PI7 6: PF4 7: PF14	Wide timer 3 Capture Compare input / output channel 1.

Alternate	LOCATION		
Functionality	0 - 3	4 - 7	Description
WTIM3_CC2	0: PD11 1: PC10 2: PC13 3: PF11	4: PI5 5: PF6 6: PF12 7: PF15	Wide timer 3 Capture Compare input / output channel 2.

Certain alternate function locations may have non-interference priority. These locations will take precedence over any other functions selected on that pin (i.e. another alternate function enabled to the same pin inadvertently).

Some alternate functions may also have high speed priority on certain locations. These locations ensure the fastest possible paths to the pins for timing-critical signals.

The following table lists the alternate functions and locations with special priority.

Table 5.5. Alternate Functionality Priority

Alternate Functionality	Location	Priority
CMU_CLK2	1: PA3 5: PD10	High Speed High Speed
CMU_CLKI0	1: PA3 5: PD10	High Speed High Speed
ETH_RMIICRSDV	0: PA4 1: PD11	High Speed High Speed
ETH_RMIIREFCLK	0: PA3 1: PD10	High Speed High Speed
ETH_RMIIRXD0	0: PA2 1: PD9	High Speed High Speed
ETH_RMIIRXD1	0: PA1 1: PF9	High Speed High Speed
ETH_RMIIRXER	0: PA5 1: PD12	High Speed High Speed
ETH_RMIITXD0	0: PE15 1: PF7	High Speed High Speed
ETH_RMIITXD1	0: PE14 1: PF6	High Speed High Speed
ETH_RMIITXEN	0: PA0 1: PF8	High Speed High Speed
QSPI0_CS0	0: PF7	High Speed
QSPI0_CS1	0: PF8	High Speed
QSPI0_DQ0	0: PD9	High Speed
QSPI0_DQ1	0: PD10	High Speed
QSPI0_DQ2	0: PD11	High Speed
QSPI0_DQ3	0: PD12	High Speed
QSPI0_DQ4	0: PE8	High Speed
QSPI0_DQ5	0: PE9	High Speed
QSPI0_DQ6	0: PE10	High Speed
QSPI0_DQ7	0: PE11	High Speed

Alternate Functionality	Location	Priority
QSPI0_DQS	0: PF9	High Speed
QSPI0_SCLK	0: PF6	High Speed
SDIO_CLK	0: PE13	High Speed
SDIO_CMD	0: PE12	High Speed
SDIO_DAT0	0: PE11	High Speed
SDIO_DAT1	0: PE10	High Speed
SDIO_DAT2	0: PE9	High Speed
SDIO_DAT3	0: PE8	High Speed
SDIO_DAT4	0: PD12	High Speed
SDIO_DAT5	0: PD11	High Speed
SDIO_DAT6	0: PD10	High Speed
SDIO_DAT7	0: PD9	High Speed
TIM0_CC0	3: PB6	Non-interference
TIM0_CC1	3: PC0	Non-interference
TIM0_CC2	3: PC1	Non-interference
TIM0_CDTI0	1: PC13	Non-interference
TIM0_CDTI1	1: PC14	Non-interference
TIM0_CDTI2	1: PC15	Non-interference
TIM2_CC0	0: PA8	Non-interference
TIM2_CC1	0: PA9	Non-interference
TIM2_CC2	0: PA10	Non-interference
TIM2_CDTI0	0: PB0	Non-interference
TIM2_CDTI1	0: PB1	Non-interference
TIM2_CDTI2	0: PB2	Non-interference
TIM4_CC0	0: PF3	Non-interference
TIM4_CC1	0: PF4	Non-interference
TIM4_CC2	0: PF12	Non-interference
TIM4_CDTI0	0: PD0	Non-interference
TIM4_CDTI1	0: PD1	Non-interference
TIM4_CDTI2	0: PD3	Non-interference
TIM6_CC0	0: PG0	Non-interference
TIM6_CC1	0: PG1	Non-interference
TIM6_CC2	0: PG2	Non-interference
TIM6_CDTI0	0: PG3	Non-interference
TIM6_CDTI1	0: PG4	Non-interference
TIM6_CDTI2	0: PG5	Non-interference

Alternate Functionality	Location	Priority
US2_CLK	4: PF8 5: PF2	High Speed High Speed
US2_CS	4: PF9 5: PF5	High Speed High Speed
US2_RX	4: PF7 5: PF1	High Speed High Speed
US2_TX	4: PF6 5: PF0	High Speed High Speed

5.5 Analog Port (APORT) Client Maps

The Analog Port (APORT) is an infrastructure used to connect chip pins with on-chip analog clients such as analog comparators, ADCs, DACs, etc. The APORT consists of a set of shared buses, switches, and control logic needed to configurably implement the signal routing. Figure 5.3 APORT Connection Diagram on page 153 Shows the APORT routing for this device family. A complete description of APORT functionality can be found in the Reference Manual.

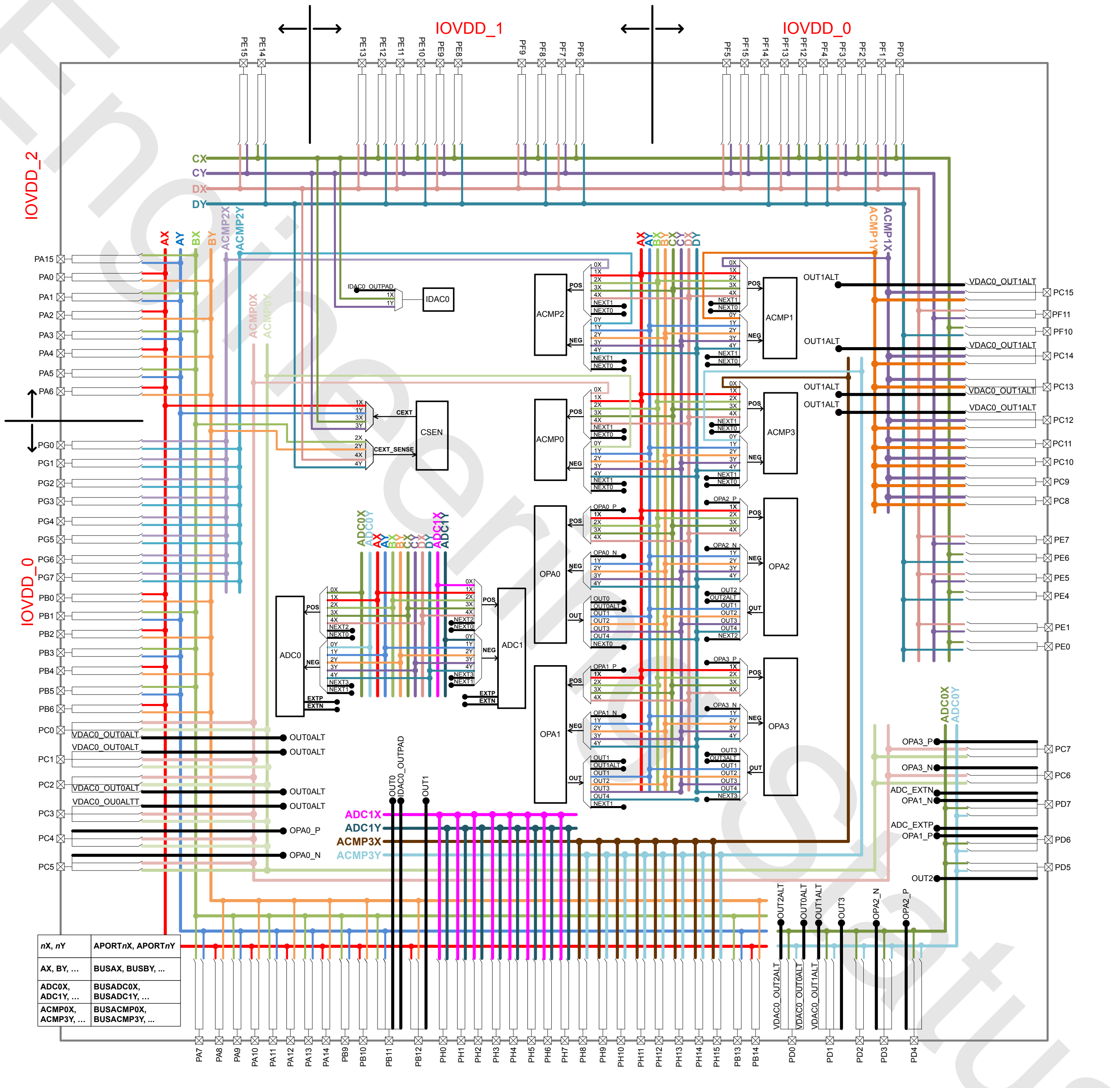


Figure 5.3. APORT Connection Diagram

Client maps for each analog circuit using the APORT are shown in the following tables. The maps are organized by bus, and show the peripheral's port connection, the shared bus, and the connection from specific bus channel numbers to GPIO pins.

In general, enumerations for the pin selection field in an analog peripheral's register can be determined by finding the desired pin connection in the table and then combining the value in the Port column (APORT__), and the channel identifier (CH__). For example, if pin PF7 is available on port APORT2X as CH23, the register field enumeration to connect to PF7 would be APORT2XCH23. The shared bus used by this connection is indicated in the Bus column.

Table 5.6. ACMP0 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT0X	BUSACMP0X																									PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
APORT0Y	BUSACMP0Y																									PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

Table 5.7. ACMP1 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT0X	BUSACMP1X																									PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
APORT0Y	BUSACMP1Y																									PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

Table 5.8. ACMP2 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT0X	BUSACMP2X																									PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0
APORT0Y	BUSACMP2Y																									PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

Table 5.9. ACMP3 Bus and Pin Mapping

APORT4Y	APORT4X	APORT3Y	APORT3X	APORT2Y	APORT2X	APORT1Y	APORT1X	APORT0Y	APORT0X	Port
BUSDY	BUSDX	BUSCY	BUSCX	BUSBY	BUSBX	BUSAY	BUSAX	BUSACMP3Y	BUSACMP3X	Bus
	PF15	PF15			PB15	PB15				CH31
PF14			PF14	PB14			PB14			CH30
	PF13	PF13			PB13	PB13				CH29
PF12			PF12	PB12			PB12			CH28
	PF11	PF11			PB11	PB11				CH27
PF10			PF10	PB10			PB10			CH26
	PF9	PF9			PB9	PB9				CH25
PF8			PF8							CH24
	PF7	PF7								CH23
PF6			PF6	PB6			PB6			CH22
	PF5	PF5			PB5	PB5				CH21
PF4			PF4	PB4			PB4			CH20
	PF3	PF3			PB3	PB3				CH19
PF2			PF2	PB2			PB2			CH18
	PF1	PF1			PB1	PB1				CH17
PF0			PF0	PB0			PB0			CH16
	PE15	PE15			PA15	PA15				CH15
PE14			PE14	PA14			PA14			CH14
	PE13	PE13			PA13	PA13				CH13
PE12			PE12	PA12			PA12			CH12
	PE11	PE11			PA11	PA11				CH11
PE10			PE10	PA10			PA10			CH10
	PE9	PE9			PA9	PA9				CH9
PE8			PE8	PA8			PA8			CH8
	PE7	PE7			PA7	PA7		PH15	PH15	CH7
PE6			PE6	PA6			PA6	PH14	PH14	CH6
	PE5	PE5			PA5	PA5		PH13	PH13	CH5
PE4			PE4	PA4			PA4	PH12	PH12	CH4
					PA3	PA3		PH11	PH11	CH3
				PA2			PA2	PH10	PH10	CH2
	PE1	PE1			PA1	PA1		PH9	PH9	CH1
PE0			PE0	PA0			PA0	PH8	PH8	CH0

Table 5.10. ADC0 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT0X	BUSADC0X																									PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
APORT0Y	BUSADC0Y																									PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

Table 5.11. ADC1 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT0X	BUSADC1X																									PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0
APORT0Y	BUSADC1Y																									PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

Table 5.12. CSEN Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
CEXT																																	
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
CEXT_SENSE																																	
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

Table 5.13. IDAC0 Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
APORT1X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT1Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	

Table 5.14. VDAC0 / OPA Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
OPA0_N																																	
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
OPA0_P																																	
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
OPA1_N																																	
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
OPA1_P																																	
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
OPA2_N																																	
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
OPA2_OUT																																	
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
OPA2_P																																	
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
OPA3_N																																	
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
OPA3_OUT																																	
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
OPA3_P																																	
APORT1X	BUSAX		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT2X	BUSBX	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT3X	BUSCX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0
APORT4X	BUSDX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
VDAC0_OUT0 / OPA0_OUT																																	
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
VDAC0_OUT1 / OPA1_OUT																																	
APORT1Y	BUSAY	PB15		PB13		PB11		PB9				PB5		PB3		PB1		PA15		PA13		PA11		PA9		PA7		PA5		PA3		PA1	
APORT2Y	BUSBY		PB14		PB12		PB10				PB6		PB4		PB2		PB0		PA14		PA12		PA10		PA8		PA6		PA4		PA2		PA0
APORT3Y	BUSCY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1		PE15		PE13		PE11		PE9		PE7		PE5				PE1	
APORT4Y	BUSDY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0		PE14		PE12		PE10		PE8		PE6		PE4				PE0

6. BGA192 Package Specifications

6.1 BGA192 Package Dimensions

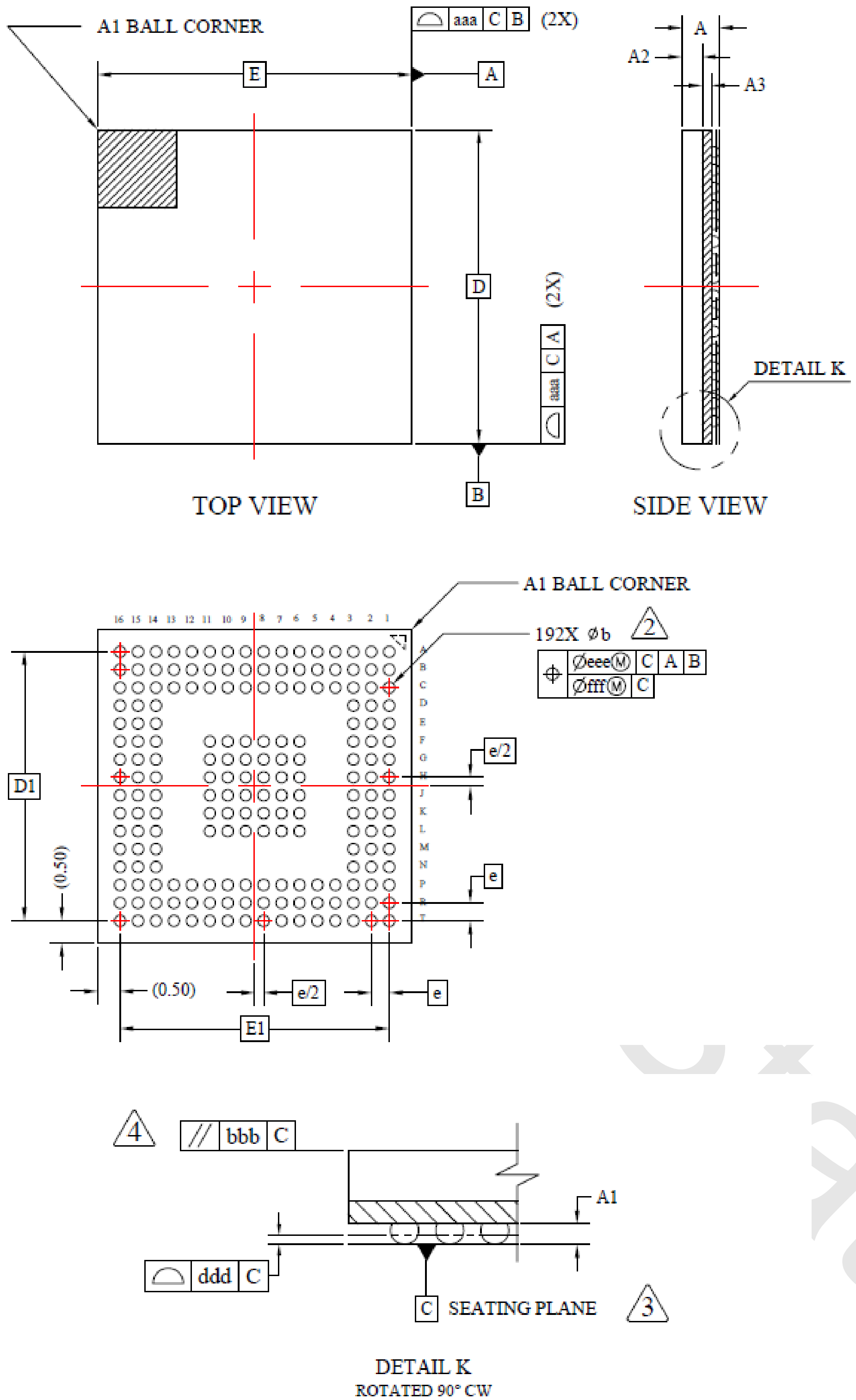


Figure 6.1. BGA192 Package Drawing

Table 6.1. BGA192 Package Dimensions

Dimension	Min	Typ	Max
A	0.77	0.83	0.89
A1	0.13	0.18	0.23
A3	0.16	0.20	0.24
A2		0.45 REF	
D		7.00 BSC	
e		0.40 BSC	
E		7.00 BSC	
D1		6.00 BSC	
E1		6.00 BSC	
b	0.20	0.25	0.30
aaa		0.10	
bbb		0.10	
ddd		0.08	
eee		0.15	
fff		0.05	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.2 BGA192 PCB Land Pattern

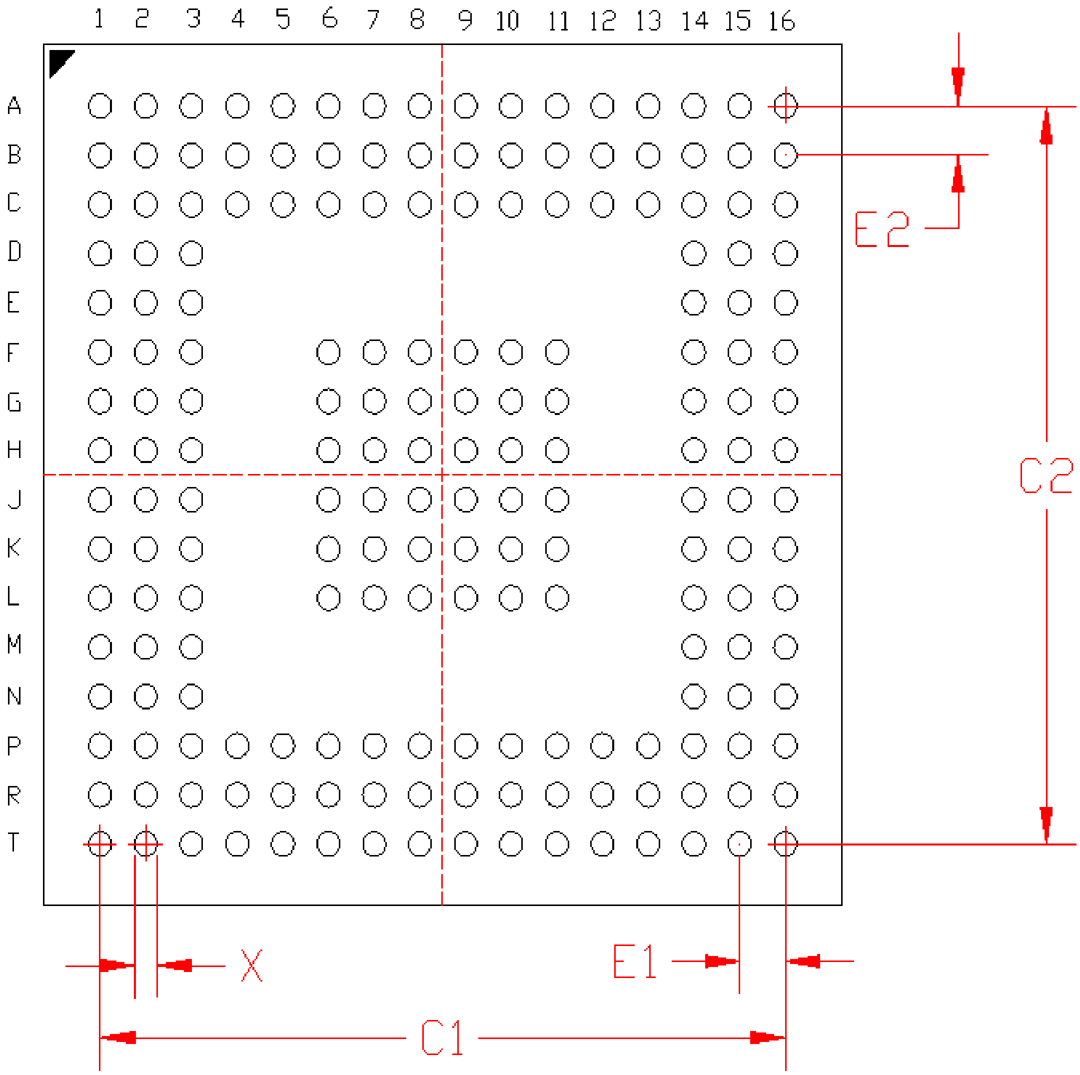


Figure 6.2. BGA192 PCB Land Pattern Drawing

Table 6.2. BGA192 PCB Land Pattern Dimensions

Dimension	Min	Nom	Max
X		0.20	
C1		6.00	
C2		6.00	
E1		0.4	
E2		0.4	

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

6.3 BGA192 Package Marking

Figure 6.3. BGA192 Package Marking

The package marking consists of:

- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

7. TQFP100 Package Specifications

7.1 TQFP100 Package Dimensions

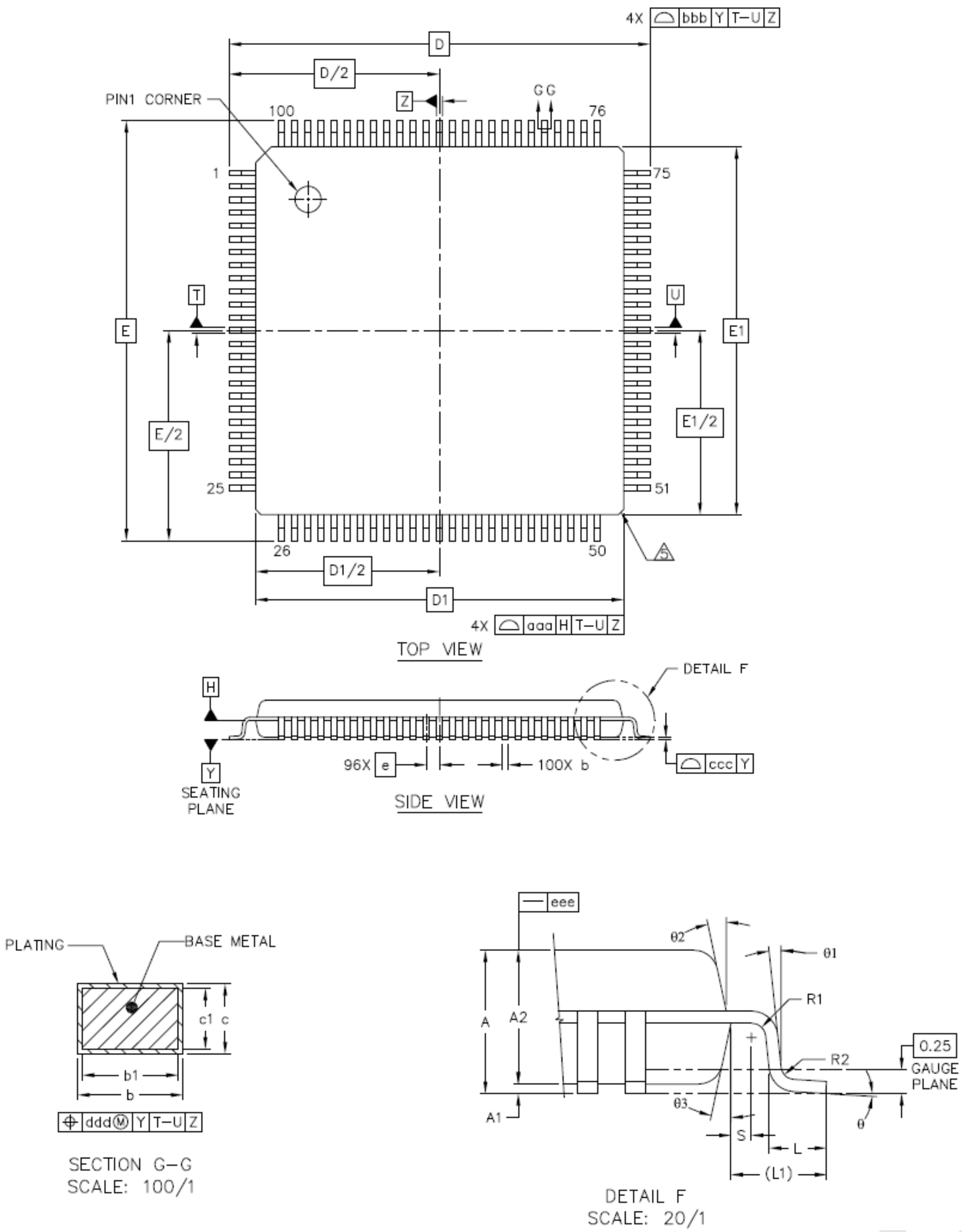


Figure 7.1. TQFP100 Package Drawing

Table 7.1. TQFP100 Package Dimensions

Dimension	Min	Typ	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	-	0.20
c1	0.09	-	0.16
D		16.0 BSC	
E		16.0 BSC	
D1		14.0 BSC	
E1		14.0 BSC	
e		0.50 BSC	
L1		1 REF	
L	0.45	0.60	0.75
Θ	0	3.5	7
Θ1	0	-	-
Θ2	11	12	13
Θ3	11	12	13
R1	0.08	-	-
R2	0.08	-	0.2
S	0.2	-	-
aaa		0.2	
bbb		0.2	
ccc		0.08	
ddd		0.08	
eee		0.05	

Note:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.2 TQFP100 PCB Land Pattern

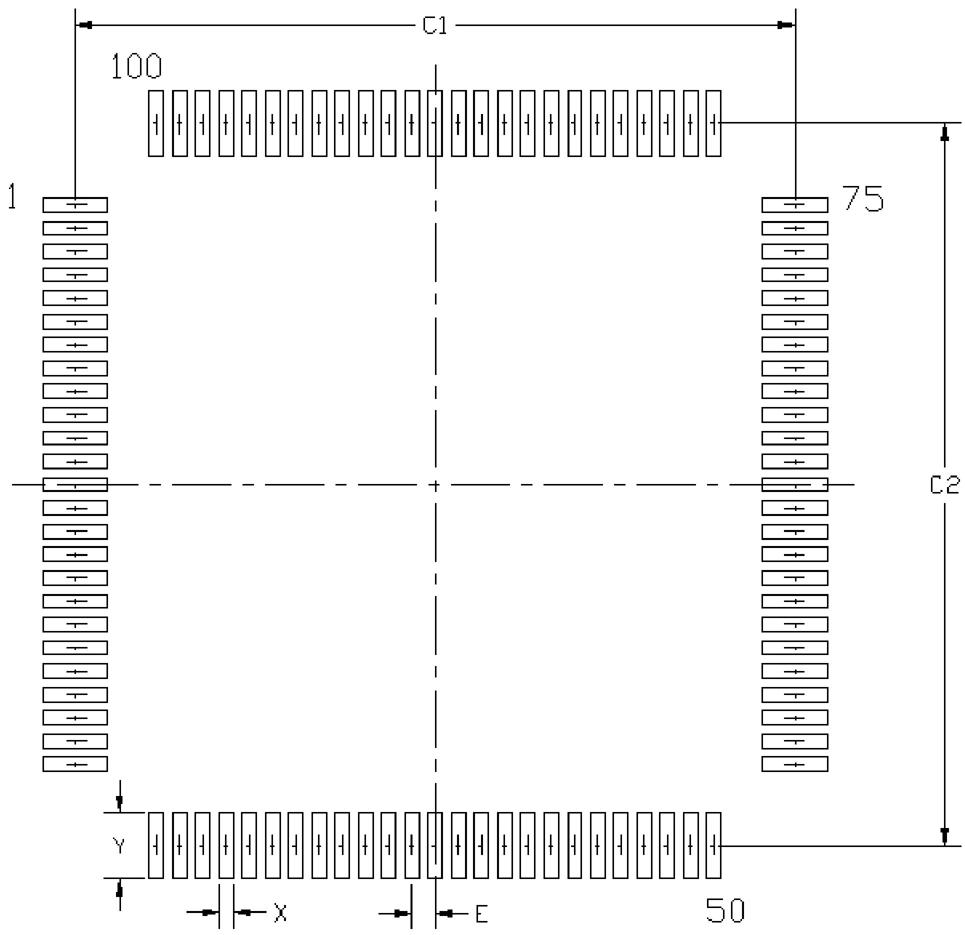


Figure 7.2. TQFP100 PCB Land Pattern Drawing

Table 7.2. TQFP100 PCB Land Pattern Dimensions

Dimension	Min	Nom	Max
C1		15.4	
C2		15.4	
E		0.50 BSC	
X		0.30	
Y		1.50	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

7.3 TQFP100 Package Marking

Figure 7.3. TQFP100 Package Marking

The package marking consists of:

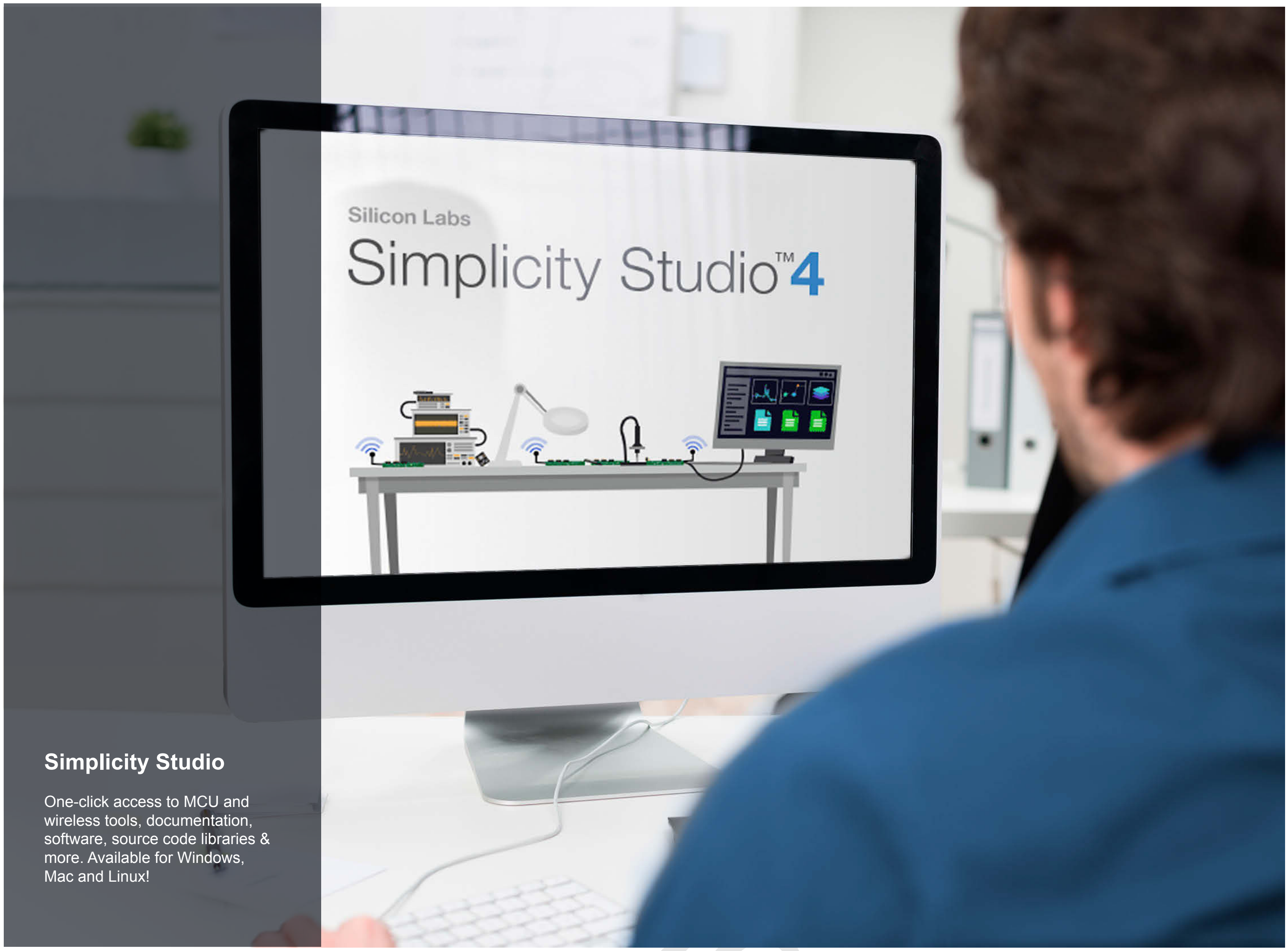
- PPPPPPPPPP – The part number designation.
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

8. Revision History

8.1 Revision 0.5

July 24th, 2017

Initial release.



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